A 3-D Generalized Direct PWM for 3-Phase 4-Wire APFs

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***Abstract*—A 3-dimensional (3D) generalized direct PWM algorithm for multilevel converters in a three-phase four-wire active power filter is proposed. It is proved to be equivalent to the newly proposed generalized 3D space vector modulation (SVM). However, the direct PWM greatly simplifies the control algorithm and is much easier to implement in digital processors. The direct PWM is applied to an active power filter, where a three-level NPC inverter is used. Important issues for implementing the DPWM in three-level inverter, such as d.c. voltage variation control and over-modulation, are discussed in detail. A d.c. voltage variation control strategy in a-b-c coordinates is also proposed. Simulation results are given to show the validity of the proposed control strategy.**

Keywords- active power filter, direct PWM, three-phase four-wire system

I. INTRODUCTION

For the medium and large capacity power quality compensators, the multi-level converters are becoming increasingly popular. It not only reduces voltage stress across the switches but also improves harmonic contents of the VSI by selecting appropriate switching vectors. The voltage stress decrease leads to corresponding decrease of dv/dt, which can reduce the electromagnetic interference (EMI).

Recently, several two-dimensional (2D) space vector modulation (SVM) methods for multilevel converter have been proposed [1]-[4]. It is necessary to extend the 2D space to the 3-dimensional (3D) space when the multilevel converter is connected to a three-phase four-wire system, because the reference vectors are not on a plane if the system is unbalanced or if there is a zero sequence or triple harmonics. Since the voltages or currents of three phases are linear independence of each other in a three-phase four-wire system, the transform between α-β-0 coordinates and a-b-c coordinates is definitely reversible. Therefore, both the two coordinates can be chosen to express the space vectors and to implement 3D SVM control.

The 3D SVM is first proposed in α-β-0 coordinates since it is natural to extend the α-β plane to α-β-0 3D coordinates [6][7]. A generalized 3D SVM in a-b-c coordinates has been proposed in 2003 [8], in which the reference voltage vector is decomposed to an offset vector and a two-level vector. Important issues for the 3DSVM, such as determination of switching sequence schemes and calculation of dwell times are all settled by a two-level 3DSVM.

In this paper, a generalized direct PWM is proposed, in which the switching state and pulse width of each phase output are directly determined according to the normalized reference voltage vector. Therefore, the time-consuming mid-steps of the 3DSVM are all avoided. It is proved that the modulation outputs of the direct PWM and the newly proposed 3D SVM in a-b-c coordinates [8] are the same when the same reference voltage vector is used. The computational cost of the direct PWM is much lower and is independent of the number of levels of the converter. So, it can be used as a generalized PWM algorithm for generating 3D control vectors.

In order to show the validity of the proposed direct PWM, it is applied to a three-phase four-wire active power filter (APF), in which a three-level neutral-point-clamped (NPC) inverter is used. One of the most important operation issues of the three-level NPC inverter is the d.c. voltage unbalance. However, most of the d.c. voltage unbalance control strategies are proposed for the SVM in α-β-0 coordinates [9]-[11]. A d.c. voltage unbalance control strategy, which is implemented by directly modifying the pulse width of each phase, is proposed in this paper. The over-modulation issue for the direct PWM is also discussed. Finally, simulation results are given to show the validity of the proposed direct PWM with d.c. voltage unbalance control.

II. GENERALIZED DIRECT PWM

An equivalent model for an N-level voltage source inverter is shown in Fig.1 [4]. The phase output voltage can be expressed as:

$$\boldsymbol{v}_j = S_j * E \qquad j=a,b,c \text{ and } 0 \le S_j \le N\text{-}1 \quad (1)$$

where $\boldsymbol{S}_j$ denotes the switching state of the corresponding phase and E denotes the d.c. voltage of one level. In this paper, all the voltage vectors are represented in per unit, i.e., normalized by E, so that the output voltage of each phase can be expressed as:

$$\boldsymbol{v}_j = S_j \qquad j=a,b,c \text{ and } 0 \le S_j \le N\text{-}1 \quad (2)$$

The reference voltage vector is normalized by E too, as expressed in (3).

$$\vec{v}_{ref} = \vec{V}_{ref} / E \qquad (3)$$

In the generalized Direct PWM, the desired output voltage vector is decomposed into two components: a offset voltage vector and a two-level voltage vector. The two-level voltage vector will be used to directly determine the final pulse width, which greatly simplifies the calculations in [8].

$$\vec{v}_{ref} = \vec{v}_{offset} + \vec{v}_{twol} \qquad (4)$$

It can also be expressed in a-b-c coordinates as:

$$\begin{bmatrix} v_{refa} \\ v_{refb} \\ v_{refc} \end{bmatrix} = \begin{bmatrix} v_{offseta} \\ v_{offsetb} \\ v_{offsetc} \end{bmatrix} + \begin{bmatrix} v_{twola} \\ v_{twolb} \\ v_{twolc} \end{bmatrix}$$

,where $\begin{bmatrix} v_{offseta} \\ v_{offsetb} \\ v_{offsetc} \end{bmatrix} = \begin{bmatrix} INT(v_{refa}) \\ INT(v_{refb}) \\ INT(v_{refc}) \end{bmatrix}$

INT( ) removes the fractional part of the real input data. If($\boldsymbol{v}_{offseta}$, $\boldsymbol{v}_{offsetb}$, $\boldsymbol{v}_{offsetc}$) equals to ($\boldsymbol{S}_a$, $\boldsymbol{S}_b$, $\boldsymbol{S}_c$), the reference voltage vector locates inside the 2-level space vector allocation formed by ($\boldsymbol{S}_a$, $\boldsymbol{S}_b$, $\boldsymbol{S}_c$), ($\boldsymbol{S}_a$+1, $\boldsymbol{S}_b$, $\boldsymbol{S}_c$), ($\boldsymbol{S}_a$, $\boldsymbol{S}_b$+1, $\boldsymbol{S}_c$), ($\boldsymbol{S}_a$, $\boldsymbol{S}_b$, $\boldsymbol{S}_c$+1), ($\boldsymbol{S}_a$+1, $\boldsymbol{S}_b$+1, $\boldsymbol{S}_c$), ($\boldsymbol{S}_a$ +1, $\boldsymbol{S}_b$, $\boldsymbol{S}_c$+1), ($\boldsymbol{S}_a$, $\boldsymbol{S}_b$+1, $\boldsymbol{S}_c$+1) and ($\boldsymbol{S}_a$ +1, $\boldsymbol{S}_b$+1, $\boldsymbol{S}_c$+1), as illustrated in Fig.2. In order to reduce the *dv*/*dt* of the output voltage in a multi-level converter, the output voltage changes only one level in one switching period. So the two switching states of one phase are $\boldsymbol{S}_j$ and $\boldsymbol{S}_j$+1 (*j=a,b,c*) in a switching period.

The direct PWM is based on the voltage second approximation just like that in conventional SVM. However, the voltage is approximated in per-phase mode in a-b-c coordinates, i.e., the reference voltage vector is synthesized in phase A, B and C independently, as illustrated in (5).

$$v_{refj} \cdot T_S = v_{offsetj} \cdot t_{offj} + (v_{offsetj} + 1) \cdot t_{onj} \quad j=a,b,c \qquad (5)$$

where T_s is the sampling period. t_{offj} is the dwell time of the output state $\boldsymbol{S}_j$. $t_{onj}$is the dwell time of the output state $\boldsymbol{S}_j$+1 and $t_{offj} + t_{onj} = T_s$ (*j=a,b,c*).

If $\boldsymbol{v}_{offsetj} \bullet T_s$ is subtracted from both sides of (5), it can be obtained:

$$(\boldsymbol{v}_{refj} - \boldsymbol{v}_{offsetj}) \bullet T_s = \boldsymbol{v}_{offsetj} \bullet t_{offj} + (\boldsymbol{v}_{offsetj}+1) \bullet t_{onj} - \boldsymbol{v}_{offsetj} \bullet (t_{offj} + t_{onj}) = t_{onj}$$

Since $\boldsymbol{v}_{refj} - \boldsymbol{v}_{offsetj} = \boldsymbol{v}_{twolj}$ *j=a,b,c* (6)

$$\boldsymbol{v}_{twolj} = t_{onj} / T_s \quad j=a,b,c \qquad (7)$$

and $1 - \boldsymbol{v}_{twolj} = t_{offj} / T_s$ (8)

The t_{onj} is just the pulse width of the corresponding phase *j* (*j=a,b,c)*, as shown in Fig.3. The normalized two-level reference voltage vector $\boldsymbol{v}_{twolj}$ in (7) equals to the normalized pulse width of the respective phase.

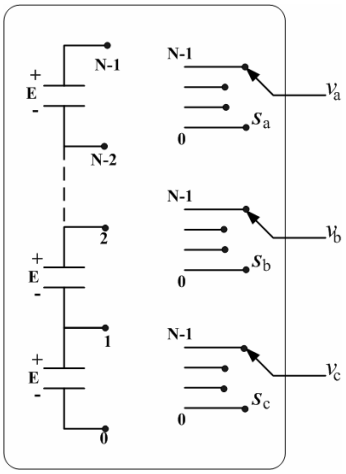

Fig.1 Equivalent model of a N-level VSI

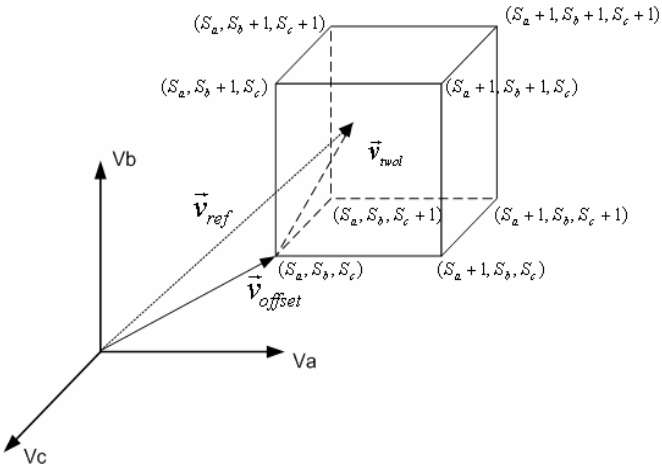

Fig.2 Decomposition of reference voltage vector

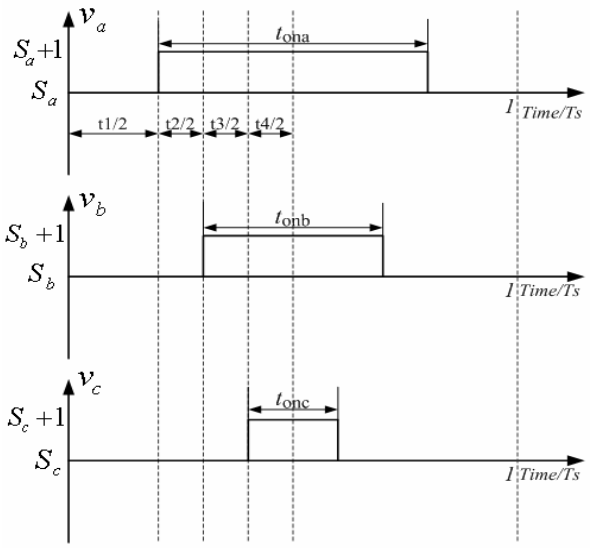

Fig.3 PWM output of one sampling period

No matter what PWM control strategies are used, the final trigger signals are sending to the switches of the respective phase independently. After the t_{onj} of each phase is determined, the modulation output of the inverter can be generated. The

proposed PWM control method is called Direct PWM because it is implemented by directly calculating the pulse width of each phase in a-b-c coordinates. This direct PWM can be easily implemented in digital processors.

III. EQUIVALENCE TO THE 3DSVM

A 3DSVM in a-b-c coordinates has been proposed in [8], in which following steps are required in order to generate final output pulses.

1) The reference voltage vector is decomposed to a offset voltage vector and a two-level voltage vector;
2) As six tetrahedrons are considered in each two-level space vectors subcube in a-b-c coordinates, the second step is to determine in which tetrahedron the two-level voltage vector is pointing. Three comparisons are needed in this part.
3) The four space vectors, which correspond to the four vertices of a tetrahedron in the selected subcube (step 2), are chosen to synthesis the two-level reference voltage vector. The dwell times of each vector is calculated.
4) The pulse width of each phase is calculated in order to generate the trigger signals of each switch.

It will be proved that step 2 to step 4 can be replaced by the calculation in (7). The reference voltage vector is synthesized by four neighboring vectors in 3DSVM as:

$$\vec{v}_{twol} \cdot T_S = \vec{v}_1 t_1 + \vec{v}_2 t_2 + \vec{v}_3 t_3 + \vec{v}_4 t_4 \qquad (9)$$

and $t_1 + t_2 + t_3 + t_4 = T_s$ (10)

Equation (9) can also be expressed as:

$$\begin{bmatrix} v_{twola} \\ v_{twolb} \\ v_{twolc} \end{bmatrix} \cdot T_S = \begin{bmatrix} S_a^1 & S_a^2 & S_a^3 & S_a^4 \\ S_b^1 & S_b^2 & S_b^3 & S_b^4 \\ S_c^1 & S_c^2 & S_c^3 & S_c^4 \end{bmatrix} \begin{bmatrix} t_1 \\ t_2 \\ t_3 \\ t_4 \end{bmatrix} \qquad (11)$$

After the dwell time of each neighboring vectors are obtained, the final output of the inverter can be generated, which is also illustrated in Fig.3. Since $\vec{v}_1$, $\vec{v}_2$, $\vec{v}_3$ and $\vec{v}_4$ are space vectors of a two-level space vector allocation, its normalized output S_j^m ($j=a, b, c$; $m=1,2,3,4$) can only be '0' or '1'.It can be found that the pulse width of each phase is just the summation of the dwell time of the vectors, whose output in that phase is equal to '1'. That is to say, if S_x^m equals to '1', the dwell time t_m of this vector $\vec{v}_m$ is added to the pulse width. If S_x^m equals to '0', the t_m is not added to the pulse width t_{onj}. So the S_x^m can also be used as the coefficients for calculating the pulse width. If phase A is considered as an example, $t_{ona} = S_a^1 t_1 + S_a^2 t_2 + S_a^3 t_3 + S_a^4 t_4$. The following equation can be obtained.

$$\begin{bmatrix} t_{ona} \\ t_{onb} \\ t_{onc} \end{bmatrix} = \begin{bmatrix} S_a^1 & S_a^2 & S_a^3 & S_a^4 \\ S_b^1 & S_b^2 & S_b^3 & S_b^4 \\ S_c^1 & S_c^2 & S_c^3 & S_c^4 \end{bmatrix} \begin{bmatrix} t_1 \\ t_2 \\ t_3 \\ t_4 \end{bmatrix} \qquad (12)$$

The (7) can be deduced again if (11) is compared with (12), which indicates that step 2 to step 4 in the 3DSVM can be replaced by the simple calculation (7). Therefore, the time-consuming mid-steps, such as neighboring vectors determination and dwell times calculation, can all be eliminated. The direct PWM and the 3DSVM generate the same output when the same reference voltage vector is applied to. However, the calculation in the direct PWM is much simpler. Furthermore, the direct PWM can be easily implemented in digital processors.

IV. IMPLEMENT DIRECT PWM IN A THREE-LEVEL APF

In order to show the validity of the proposed direct PWM, it is applied to a three-phase four-wire APF, in which a three-level NPC inverter is used. The three-level neutral point clamped (NPC) inverter has been used in APFs for a three-phase three-wire system. If a wire is connected between the system neutral and the mid-point of the d.c. capacitors, the three-level NPC inverter can also be utilized in a three-phase four-wire system without modifying its structure, as shown in Fig.4. Compared with three-level four-leg NPC inverter, the three-leg NPC inverter uses less switching components and its initial cost is lower. Furthermore, there are totally 81 vectors of a three-level four-leg inverter, which greatly increases the complexity of the PWM control. So the three-leg NPC inverter is chosen in this paper. When the direct PWM is implemented, some important operation issues should be considered first.

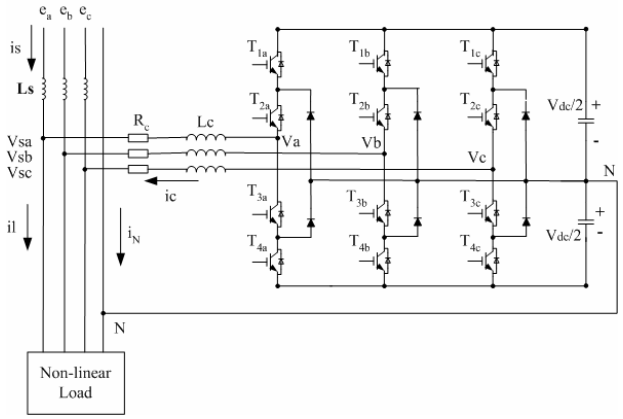

Fig.4 System configuration of a three-phase four-wire active power filters

A. D.C. voltage unbalance control

One of the most important operation issues for a three-level NPC inverter is d.c. voltage unbalance. The unbalance between the two d.c. capacitors must be controlled because large d.c. unbalance not only affects the compensation performance but also causes potential system unstable.

The output voltage vector of the inverter in a-b-c coordinates is expressed as:

$$\vec{v} = \sqrt{\frac{2}{3}}\left(S_a + \alpha \cdot S_b + \alpha^2 \cdot S_c\right) \qquad (13)$$

where $\alpha = e^{j\frac{2\pi}{3}}, \alpha^2 = e^{-j\frac{2\pi}{3}}$

According to the α-β-0 transformation as shown in (14), the instantaneous voltage vector in α-β-0 frame is given as (15).

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} \qquad (14)$$

$$\vec{v} = \left(v_\alpha \cdot \vec{n}_\alpha + v_\beta \cdot \vec{n}_\beta + v_0 \cdot \vec{n}_0\right) \qquad (15)$$

If ($\boldsymbol{S}_a$, $\boldsymbol{S}_b$, $\boldsymbol{S}_c$) and ($\boldsymbol{S}_a$+1, $\boldsymbol{S}_b$+1, $\boldsymbol{S}_c$+1) are substituted to (14), results indicate that the α- and β-axes output of the two vectors are the same, and only their zero-axis outputs are different [10].

It is assumed that the d.c. voltage across each capacitor is larger than the peak value of the phase-to-neutral voltage at the point of common coupling. The d.c. voltage variations corresponding to the switching state of one leg are illustrated in Fig.5. If S_j=2, V_{dc1} decreases. If S_j=0, V_{dc2} decreases. If S_j=1, the output of this leg is connected to the mid-point of the d.c. capacitors. The current of this phase does not passing through either of the d.c. capacitors. The switching states of the three legs together determine the variations of the voltage across the d.c. capacitors [11].

In order to reduce the switching losses, the switching state of each leg can only change one level in one sampling period. Hence, the dwell times of the vectors ($\boldsymbol{S}_a$, $\boldsymbol{S}_b$, $\boldsymbol{S}_c$) and ($\boldsymbol{S}_a$+1, $\boldsymbol{S}_b$+1, $\boldsymbol{S}_c$+1) will be varied to control the d.c. voltage unbalance. Although this method does not have the largest d.c. voltage unbalance control capability, it gives a good compromise between the switching losses and the d.c. voltage unbalance control. The compensation performance on α- and β-axes is not affected by the d.c. voltage unbalance control. Only the compensation in zero-axis is affected [10].

The dwell time of ($\boldsymbol{S}_a$+1, $\boldsymbol{S}_b$+1, $\boldsymbol{S}_c$+1) is just the minimum pulse width among three phases, as shown in Fig.3. In the proposed d.c. voltage unbalance control strategy, the pulse width of each phase is changed according to (16).

$$\boldsymbol{t}_{onj} = \boldsymbol{t}_{onj} - \boldsymbol{t}_{change} \qquad j=a,b,c \qquad (16)$$

,where $\boldsymbol{t}_{change} = \boldsymbol{t}_{min} \bullet k \bullet (V_{dc1} - V_{dc2})/E$ (17)

$$\boldsymbol{t}_{min} = \text{minimum}\,(\boldsymbol{t}_{ona}, \boldsymbol{t}_{onb}, \boldsymbol{t}_{onc})$$

and k is the gain of the feedback loop.

Since the pulse widths of three phases are modified with the same value, only the dwell times of vectors ($\boldsymbol{S}_a$, $\boldsymbol{S}_b$, $\boldsymbol{S}_c$) and ($\boldsymbol{S}_a$+1, $\boldsymbol{S}_b$+1, $\boldsymbol{S}_c$+1) are modified. The d.c. voltage unbalance control is implemented by varying the pulse width in a-b-c coordinates. A larger value of k has a larger d.c. voltage unbalance control capability. However, the $\boldsymbol{t}_{change}$ can't be larger than the $\boldsymbol{t}_{min}$. Hence, a proper k value should be chosen according to the system parameters.

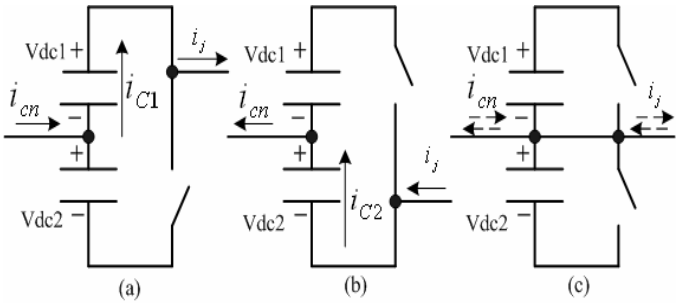

Fig. 5 D.C. capacitors voltage variation (a) S_j=2 (b) S_j=0 (c) S_j=1

B. Over-modulation

The output voltage of each phase is limited by the d.c. voltage across each d.c. capacitor. In a three-level inverter, the reference voltage should be restricted between $0 \sim 2V_{dc}$.

$$0 \le \boldsymbol{v}_{refj} \le 2V_{dc} \quad j=a,b,c \qquad (18)$$

The following modifications are adopted when $\boldsymbol{v}_{refj}$ exceeds this range.

$$\boldsymbol{v}_{refj} = 2V_{dc} \quad \text{if } \boldsymbol{v}_{refj} > 2V_{dc} \qquad (19)$$

$$\boldsymbol{v}_{refj} = 0 \quad \text{if } \boldsymbol{v}_{refj} < 0 \qquad (20)$$

The pulse widths of each phase are restricted between $0 \sim T_s$, which is always satisfied if no d.c. voltage unbalance control is applied. However, the pulse width may have been changed by the d.c. voltage variation control strategy, as illustrated in (16). Hence, the pulse widths need to be compared with the boundary conditions and to be modified again.

$$\boldsymbol{t}_{onj} = T_S \quad \text{if } \boldsymbol{t}_{onj} > T_S \qquad (21)$$

$$\boldsymbol{t}_{onj} = 0 \quad \text{if } \boldsymbol{t}_{onj} < 0 \qquad (22)$$

After the comparisons in (19) ~ (22) are done and the corresponding modifications are made, the proper direct PWM output of the inverter can be generated.

The final flow chart of the direct PWM is shown in Fig.6.

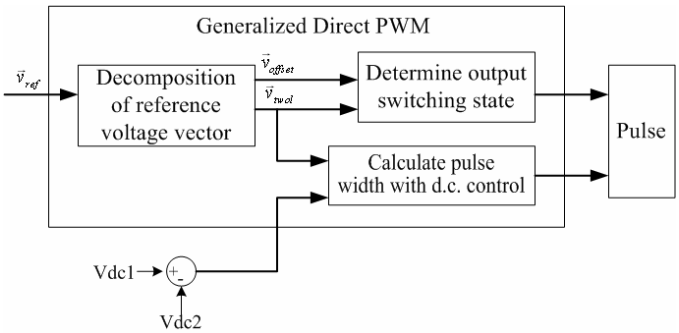

Fig.6 Flow chart of direct PWM method

V. Simulation Results

The proposed direct PWM is applied to a three-phase four-wire active power filter (APF) with 5kHz sampling frequency. The system configuration is shown in Fig.4. The simulation is done by using Matlab/Simulink. The three-phase unbalanced non-linear loads are used. The peak value of the source voltage

is 100V and Rc=2Ω, Lc=12mH, V_{dc}=160V. The proposed d.c. voltage variation control strategy is also achieved, where the coefficient *k* is chosen to be *-8*.

The load current is shown in Fig.7. The source current is shown in Fig.8 when the direct PWM with d.c. voltage variation control is applied. The APF begins to compensate at 0.02s. The d.c. voltage without any control and after being controller are shown in Fig.9 and Fig.10 respectively.

It can be seen that the source current harmonics, current unbalance and neutral current can be compensated simultaneously. The APF can trace the variation in the load current dynamically. The d.c. voltage unbalance can also be controlled by using the proposed direct PWM with d.c. voltage unbalance control. The total harmonic distortion (THD) values of the three-phase currents are listed in Table 1. The THD values indicate that the compensation performance is slightly affected after the d.c. voltage unbalance control strategy is added to the direct PWM control.

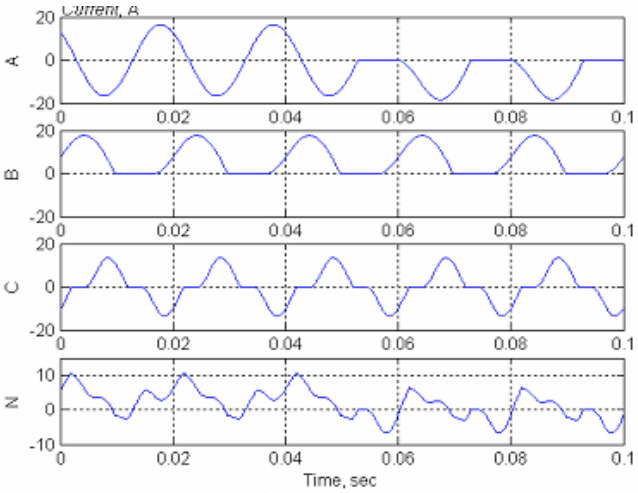

Fig.7 Load Currents

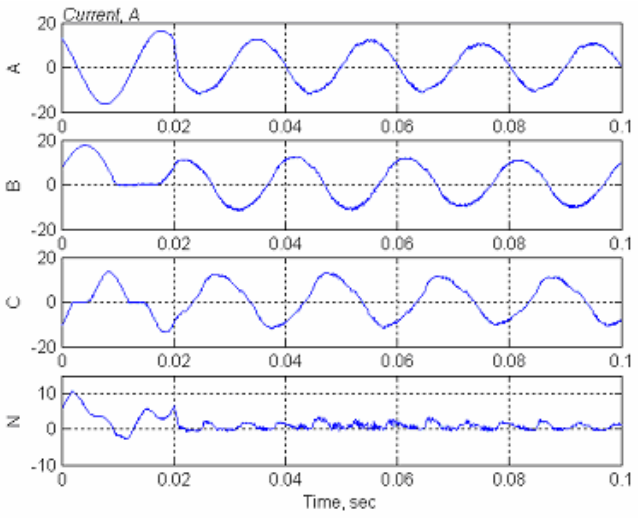

Fig. 8 Source current after compensation by direct PWM

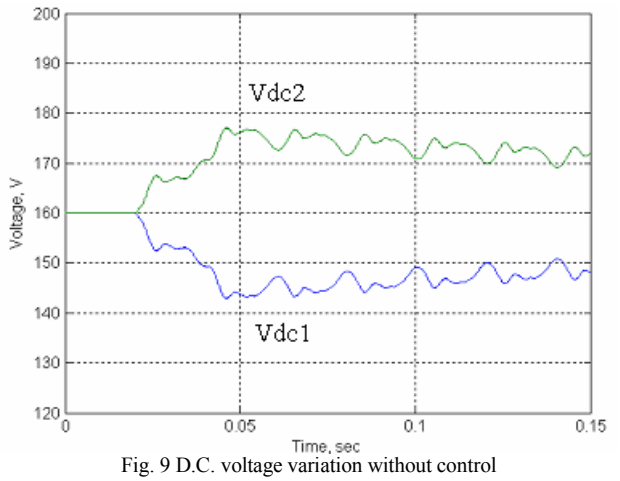

Fig. 9 D.C. voltage variation without control

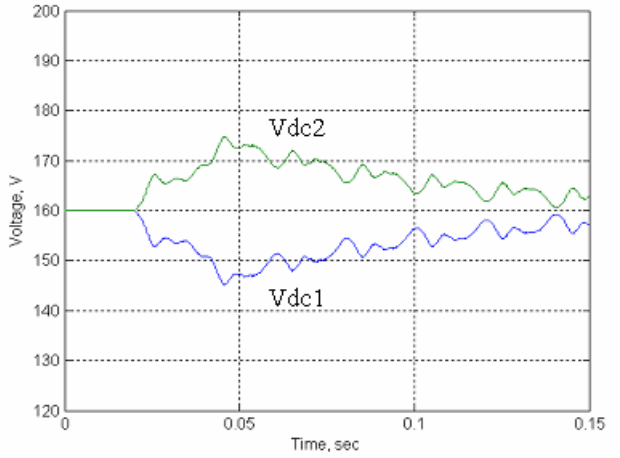

Fig.10 D.C. voltage variation after controlled

TABLE I. THD VALUES

	A	B	C
Before Compensation	28.5%	28.5%	35.68%
Direct PWM without d.c. control	4.595%	4.663%	8.016%
Direct PWM with d.c. control	5.281%	4.989%	8.757%

VI. CONCLUSIONS.

In this paper, a generalized direct PWM control strategy is proposed. It is proved to be equivalent to the 3DSVM in a-b-c coordinates. However, the time-consuming mid-steps calculations in the 3DSVM can all be simplified to one equation in the direct PWM, which greatly simplifies the PWM control. The computational complexity of the proposed direct PWM is always the same for inverters of different levels and it can be easily implemented in digital controllers. The direct PWM is applied to a three-phase four-wire active power filter, in which a three-level NPC inverter is used. A novel d.c. voltage unbalance control strategy is also proposed, which is achieved by modifying the pulse width in a-b-c coordinates. Finally, simulation results are given to show the validity of the proposed direct PWM with d.c. voltage unbalance control.

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