A FPGA-Based Generalized Pulse Width Modulator for Three-Leg Center-Split and Four-Leg Voltage Source Inverters

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***Abstract*—In this paper, a generalized pulse width (PW) modulator is proposed which can control three-leg center-split voltage source inverters (VSIs) and four-leg VSIs from two-level to multilevel topologies. VSIs with a neutral wire connection are important for power electronics applications in three-phase four-wire systems, such as active power filters and uninterruptible power supplies. For medium and large capacity applications, a multilevel three-phase four-wire VSI is a good alternative to a two-level one. However, implementing the pulse width modulation for three-phase four-wire VSIs involves complex calculations, and control algorithms differ for VSIs of different levels and topologies. The proposed generalized PW modulator controls VSIs based on voltage-second approximation, but its implementation is much easier than space vector modulation. Field programmable gate array has been chosen to implement the PW modulator due to its fast prototyping, simple hardware, and software design. Simulation and experimental results are provided. The proposed generalized PW modulator was also applied to the control system of three-phase four-wire active power filters to show its validity.**

***Index Terms*—Active power filter, four-leg voltage source inverter, three-leg center-split voltage source inverter (VSI), three-phase four-wire.**

I. Introduction

In the past, a three-phase four-wire circuit was the circuit of choice in low voltage distribution systems. Recently, it was selected by most utilities in North America as the medium voltage distribution system even though many utilities started with a three-wire ungrounded delta system [1], [2]. Voltage source inverters (VSIs) with a neutral wire connection are important for power electronics applications in three-phase four-wire distribution systems [3]–[7]. The pulse width (PW) modulator controls the VSIs to generate the required voltages or currents according to the references, as illustrated in Fig. 1. If a generalized PW modulator is available for controlling the three-phase four-wire VSIs of different topologies and levels, much effort and time can be saved in implementing pulse width modulation (PWM) in different applications.

Three-phase VSIs have two ways of providing a neutral connection for three-phase four-wire systems: 1) using split dc-linked capacitors and tying the neutral point to the mid-point of the dc linked capacitors [4]–[6] and 2) using a four-leg inverter topology and tying the neutral point to the mid-point of the fourth neutral leg [8]–[10]. For medium and large capacity applications, a multilevel three-phase VSI is a better solution than a two-level one [11]–[13]. Topologies of three-leg center-split VSIs and four-leg VSIs are shown in Fig. 1.

Comparisons were carried out between three-leg center-split VSIs and four-leg VSIs [14], [15]. The two-level four-leg inverter is preferred in low-voltage applications, especially when large neutral currents need to be manipulated. However, multilevel three-leg center-split VSIs are more preferable than four-leg VSIs in medium and large capacity applications due to lower initial cost and fewer switching devices that need to be controlled.

In a three-phase four-wire system, the reference vector is not on the $\alpha - \beta$ plane if the system is unbalanced, or if there is a zero sequence or triple harmonics [16]. As a result, the PWM methods of three-phase four-wire VSIs are realized in a 3-D space. The 3-D hysteresis PWM was first proposed for two-level three-phase four-wire VSIs in 1997 [4]. The 3-D hysteresis PWM methods for three-level VSIs were also proposed [17], [18], which involve complicated switching tables.

The space vector modulation (SVM) is based on voltage-second approximation. It reduces commutation losses and harmonic contents of output voltages, and provides more efficient use of supply voltages in comparison with the hysteresis PWM. The generalized 3-D SVM methods of multilevel three-leg center-split VSIs were proposed [15], [19], in which the multilevel 3-D SVM is simplified to a two-level case by decomposing the reference voltage. The 3-D SVM methods of two-level four-leg inverters were also proposed [9], [20], but up to now, 3-D SVM for multilevel four-leg VSIs has not been developed. Although much progress has been made, SVM for three-phase four-wire VSIs still involves complex calculations. In addition, implementing PWM for each specific three-phase four-wire VSI in different applications is a time-consuming task for most researchers.

Many researches chose to implement PWM by digital signal processor (DSP) or microcontroller (MCU). This approach has

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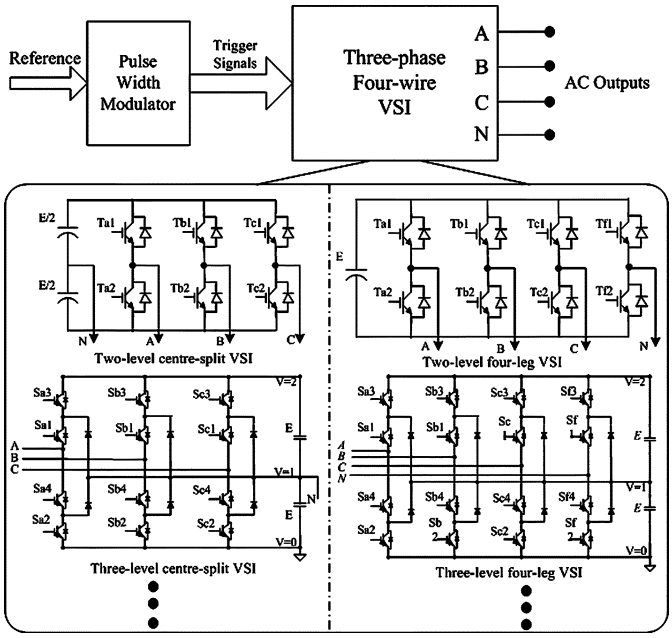


Fig. 1. Three-phase four-wire voltage source inverters.

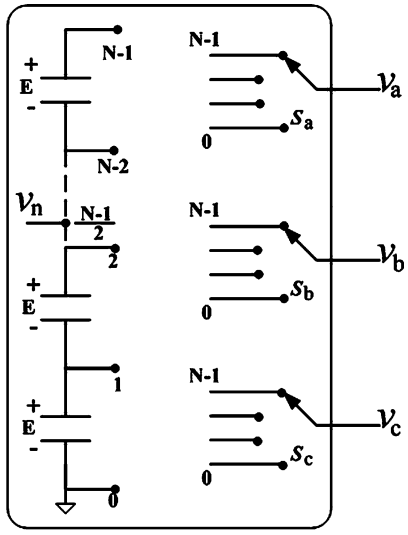


Fig. 2. Equivalent model of a three-leg N-level VSI.

the advantages of simple circuitry, software realization and flexibility. However, there are also several disadvantages [21], [22].

- As the levels of the inverter increase and the inverter structure becomes more complex, the programming of the corresponding PWM in the DSP or MCU becomes one of the most time-consuming tasks.
- If the DSP or MCU is not able to provide enough on-chip peripherals, such as comparators and dead-time controllers to support the PWM outputs, extra hardware circuits need to be designed to cooperate with the controller.

An attractive idea is to implement the PWM via an application-specific integrated circuit (ASIC). The field programmable gate array (FPGA) is a sub-class of ASIC controllers which provides characteristics such as fast prototyping, simple hardware and software design and higher switching frequency [23], [24]. The FPGA-based SVM ICs for a two-level three-phase three-wire inverter were proposed [25], [26]. The FPGA-based PW modulators for multilevel three-phase three-wire VSIs were also developed [27]–[29]. However, a generalized PW modulator for three-phase four-wire VSIs remains an unexplored area.

In this paper, a 3-D direct PWM is first proposed for multilevel three-leg center-split VSIs in order to simplify the complex algorithms of SVM. The 3-D direct PWM inherits the merits of SVM, such as a constant switching frequency and low output ripples. Another important merit of the proposed 3-D direct PWM is that it can also control the four-leg VSIs by introducing a shifting voltage to modify the references. Simulation results are provided to show the validity of the proposed 3-D direct PWM.

Based on the proposed 3-D direct PWM, a FPGA-based generalized PW modulator is developed in this paper, which can be applied to control three-leg center-split VSIs and four-leg VSIs from two-level to multilevel topologies. Prototypes were built and experimental results have been provided to show its validity. The FPGA-based PW modulator also cooperates with a DSP to control active power filters (APF), in which a two-level four-leg VSI and a three-level three-leg center-split VSI are used respectively. Again, experimental results have been provided to show that current harmonics, reactive currents and neutral currents can be simultaneously compensated by using the proposed generalized PW modulator.

II. 3-D Direct PWM of Three-Leg Center-Split VSIs

The SVM for a multilevel inverter involves complex tables of vectors and awkward mathematical relationships. A generalized 3-D SVM was proposed for multilevel three-leg center-split VSIs [16], in which the multilevel 3-D SVM issue is simplified to a two-level 3-D SVM by decomposing the reference vector. Based on voltage-second approximation, the reference voltage vector is synthesized by four neighbouring vectors which are chosen among eight available two-level vectors. The dwell time of each vector in one control period is calculated. The final PWM outputs are generated according to the neighbouring vectors and their dwell times. In order to simplify the control algorithm of SVM, 3-D direct PWM is proposed in which the reference voltage is still synthesized based on voltage-second approximation. However, the PW of each phase is directly determined according to the reference voltages. The equivalence between the 3-D direct PWM and the 3-D SVM is proved in the Appendix of this paper. The 3-D direct PWM of multilevel three-leg center-split VSIs is proposed from here on.

A. Normalization of Voltage Vectors

An equivalent model for an N-level three-leg center-split VSI is shown in Fig. 2.

The output voltage of each leg is expressed as

$$V_j = E * S_j \quad j = a, b, c \tag{1}$$

where E is the voltage of one level, and S_j is the switching function. For an N-level inverter, the value of S_j varies among 0 to $N-1$, and the dc bus voltage equals $(N-1)E$. When the N-level three-leg inverters are applied to a three-phase four-

wire system, the neutral wire is connected to the mid-point of the dc bus. Hence, the voltage v_n in reference to the virtual ground in Fig. 2 is expressed as

$$V_n = E * (N-1)/2. \tag{2}$$

All the voltages are expressed per unit, i.e., normalized by E, so that the output voltage of each leg has the same value as the switching function S_j

$$v_j = S_j \quad j = a, b, c \tag{3}$$

and

$$v_n = (\mathrm{N} - 1)/2. \tag{4}$$

Normalization facilitates the following steps in the proposed 3-D direct PWM. The phase-to-neutral reference voltages are also normalized by E, as given in (5). v_n is added to the reference voltages, so that both the output voltages of the inverter and the reference voltages are in reference to the same virtual ground

$$\vec{v}_{\mathrm{ref}} = \vec{V}_{\mathrm{ref}}/E + V_n/E = \begin{bmatrix} V_{af}/E \\ V_{bf}/E \\ V_{cf}/E \end{bmatrix} + \frac{N-1}{2}. \tag{5}$$

B. Decomposition of Reference Voltage Vector

In the 3-D direct PWM, the reference voltage vector is first split into two components as

$$\vec{v}_{\mathrm{ref}} = \vec{v}_{\mathrm{offset}} + \vec{v}_{\mathrm{twol}}. \tag{6}$$

The offset component of the reference voltage is defined in the a-b-c coordinates as

$$\vec{v}_{\mathrm{offset}} = \begin{bmatrix} v_{\mathrm{offseta}} \\ v_{\mathrm{offsetb}} \\ v_{\mathrm{offsetc}} \end{bmatrix} = \begin{bmatrix} \mathrm{Int}(v_{\mathrm{refa}}) \\ \mathrm{Int}(v_{\mathrm{refb}}) \\ \mathrm{Int}(v_{\mathrm{refc}}) \end{bmatrix} \tag{7}$$

where $\mathrm{Int}()$ removes the fractional part of the real input data. Consequently, the two-level component of the reference voltage is the fractional part

$$\vec{v}_{\mathrm{twol}} = \vec{v}_{\mathrm{ref}} - \vec{v}_{\mathrm{offset}} = \begin{bmatrix} v_{\mathrm{twola}} \\ v_{\mathrm{twolb}} \\ v_{\mathrm{twolc}} \end{bmatrix} \tag{8}$$

where $0 \le v_{\mathrm{twol}(j)} < 1 (j = a, b, c)$.

If $(v_{\mathrm{offseta}}, v_{\mathrm{offsetb}}, v_{\mathrm{offsetc}})$ equals (S_a, S_b, S_c), the reference voltage vector must be located inside a two-level space vector allocation formed by vectors: $(S_a, S_b, S_c), (S_a + 1, S_b, S_c), (S_a, S_b + 1, S_c), (S_a, S_b, S_c + 1), (S_a + 1, S_b + 1, S_c), (S_a + 1, S_b, S_c + 1), (S_a, S_b + 1, S_c + 1)$ and $(S_a + 1, S_b + 1, S_c + 1)$.

C. Determine the PW of Each Phase

In order to reduce the switching losses and the output ripples, the output voltage of each leg changes only one level in one period. Therefore, determining the dwell times of the two switching states $\boldsymbol{v}_{\mathrm{offsetj}}$ and $\boldsymbol{v}_{\mathrm{offsetj}} + 1$ can generate the PWM outputs in every period. The dwell time of $\boldsymbol{v}_{\mathrm{offsetj}} + 1 (j = a, b, c)$ is calculated by voltage-second approximation in per-phase mode, i.e., the reference voltage is synthesized in phases A, B, and C independently

$$v_{\mathrm{refj}} \cdot 1 = v_{\mathrm{offsetj}} \cdot t_{\mathrm{offj}} + (v_{\mathrm{offsetj}} + 1) \cdot t_{\mathrm{onj}} \quad j = a, b, c \tag{9}$$

$$t_{\mathrm{off}} + t_{\mathrm{onj}} = 1 \quad j = a, b, c \tag{10}$$

t_{offj} is the dwell time of the output state $\boldsymbol{v}_{\mathrm{offsetj}}$, and t_{onj} is the dwell time of $\boldsymbol{v}_{\mathrm{offsetj}} + 1$. Both t_{offj} and t_{onj} are already normalized by T_s which is the period for generating PWM outputs. Equation (11) is obtained by subtracting $\boldsymbol{v}_{\mathrm{offsetj}}$ from both sides of (9)

$$\begin{aligned}(v_{\mathrm{refj}} - v_{\mathrm{offsetj}}) &= v_{\mathrm{offsetj}} \cdot t_{\mathrm{offj}} \\ &\quad + (v_{\mathrm{offsetj}} + 1) \cdot t_{\mathrm{onj}} \\ &\quad - v_{\mathrm{offsetj}} \cdot (t_{\mathrm{offj}} + t_{\mathrm{onj}}) = t_{\mathrm{onj}}.\end{aligned} \tag{11}$$

Since $v_{\mathrm{refj}} - v_{\mathrm{offsetj}} = v_{\mathrm{twolj}} (j = a, b, c)$, it can be concluded that

$$t_{\mathrm{onj}} = v_{\mathrm{twolj}} \quad j = a, b, c \tag{12}$$

and

$$t_{\mathrm{offj}} = 1 - v_{\mathrm{twolj}} \quad j = a, b, c. \tag{13}$$

Equation (12) indicates that the normalized two-level reference voltage is equal to the normalized PW of the corresponding phase.

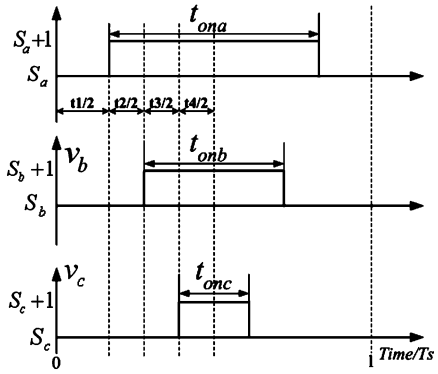


Fig. 3. PWM output of one control period.

D. Generate PWM Outputs

After the PW of each phase is calculated, the final modulation outputs are generated, as illustrated in Fig. 3. The symmetrically aligned scheme is chosen because it gives the lowest output voltage distortion and current ripples [9]. In the proposed 3-D direct PWM, $v_{\mathrm{offset}j} (j = a, b, c)$, the integer part of the normalized reference voltage, determines the switching patterns S_j and $S_j + 1$; $v_{\mathrm{two}lj} (j = a, b, c)$; the fractional part of the reference voltage, is equal to the normalized PW t_{onj} in Fig. 3.

It is mentioned in [19] that sixty-nine instructions and a maximum of three comparisons are needed for calculating 3-D state

vectors and duty-cycles in the 3-D SVM. However, only nine instructions and zero comparisons are needed to calculate the PWs in the proposed 3-D direct PWM.

III. 3-D Direct PWM of Four-Leg VSIs

Besides three-leg center-split VSIs, four-leg VSIs are also widely used in applications in three-phase four-wire systems. The 3-D SVM for two-level four-leg inverters was proposed in 2002 [9], in which the reference voltage vectors are synthesized by three neighbouring vectors and two net zero vectors in one PWM period. There are a total of 24 different neighbouring vector combinations for a two-level four-leg VSI, and each one has its own dwell-time determination matrix for calculating the dwell times of neighbouring vectors. Therefore, the 3-D SVM of a two-level four-leg inverter involves complex calculations and switching tables.

A carrier-based PWM was proposed for two-level four-leg VSIs which was proved to be equivalent to the 3-D SVM [30]. The basic idea of the carrier-based PWM is to generate the PWM outputs by direct determining the PW of each leg according to its reference voltage. A shifting voltage is introduced in the carrier-based PWM to determine the reference voltages for each leg of a four-leg VSI. The 3-D direct PWM is also based on generating the pulse of each leg independently. Therefore, the 3-D direct PWM can be considered in its application to four-leg inverters and is proposed in this section.

A. Effective Time

The output phase-to-neutral voltages of two-level four-leg VSIs are determined by the difference between the output voltages of leg $j(j = a, b, c)$ and the fourth-leg f

$$v_{jf} = v_{\text{refj}} - v_{\text{reff}} \quad j = a, b, c. \tag{14}$$

According to the 3-D direct PWM, the normalized PW of each leg is equal to the normalized two-level reference voltage, as given in (15). If (14) is substituted to (15), the PWs of legs A, B and C are expressed as (16)

$$t_{\text{onj}} = v_{\text{refj}} + 1/2 \quad j = a, b, c, f \tag{15}$$

$$t_{\text{onj}} = v_{\text{jf}} + v_{\text{reff}} + 1/2 \quad j = a, b, c. \tag{16}$$

The $v_{jf}(j = a, b, c)$ is the phase-to-neutral reference voltage for controlling four-leg VSIs. Combining (15) and (16), we find that v_{ff} should always equal zero if (17) is used to calculate the dwell time of each leg

$$t_{\text{onj}} = v_{jf} + v_{\text{reff}} + 1/2 \quad j = a, b, c, f. \tag{17}$$

The corresponding output pulses of a two-level four-leg inverter are shown in Fig. 4. The rising-edge aligned scheme was chosen for the convenience in illustrating the effective time in the following discussions.

The effective time is defined as (18), which equals the difference between the dwell times of legs A, B, or C and the fourth leg f, as shown in Fig. 4. If (17) is substituted by (18), (19) indicates that output phase-to-neutral voltages are generated in

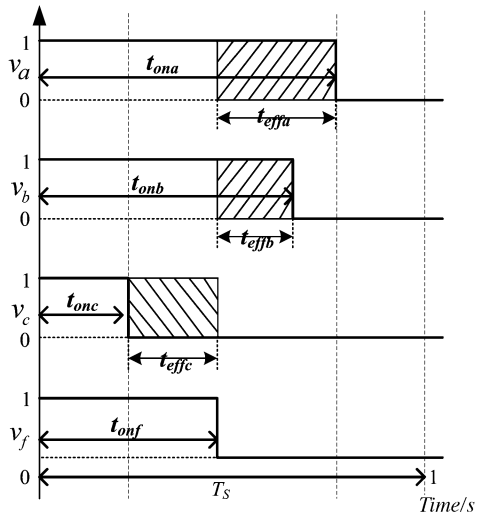


Fig. 4. Output PWs and effective times.

dwell time t_{effj}. In addition, the effective time t_{effj} is equal to the normalized phase-to-neutral voltage

$$t_{\text{effj}} = t_{\text{onj}} - t_{\text{onf}} \quad j = a, b, c \tag{18}$$

$$t_{\text{effj}} = t_{\text{onj}} - t_{\text{onf}} = v_{jf} + v_{\text{reff}} + 1/2 - (v_{\text{reff}} + 1/2) = v_{jf}. \tag{19}$$

B. Shifting Voltage

Only the reference voltage v_{reff} of the fourth-leg is unknown when the PW of each leg is calculated by (17). According to (19), the variation of the v_{reff} does not affect the output phase-to-neutral voltages of a four-leg VSI. Hence, the v_{reff} can be freely chosen if the condition in (20) is satisfied, which limits the normalized PWs in the range of 0 to 1

$$0 < v_{jf} + v_{\text{reff}} + 1/2 < 1 \quad j = a, b, c, f. \tag{20}$$

Equation (20) can be rewritten as

$$-1/2 - v_{\min} < v_{\text{reff}} < 1/2 - v_{\max} \tag{21}$$

where $V_{\max}$ is defined as the maximum number from among $v_{af}, v_{bf}, v_{cf}, v_{ff}$; and is the minimum number from among $v_{af}, v_{bf}, v_{cf}, v_{ff}$. Equation (21) only provides the range for v_{reff}. In order to get a fixed value for v_{reff}, an extra constraint is adopted.

Besides the effective time for generating output voltages, there are redundant times in one PWM period which are taken up by the switching states (0,0,0,0) and (1,1,1,1). The output phase-to-neutral voltages are zero when the four-leg VSI operates according to the two switching patterns. It is assumed that the dwell times of states (0,0,0,0) and (1,1,1,1) are the same, so that the optimal switching sequence can be achieved. Consequently, (22) is obtained

$$t_{\text{on min}} = 1 - t_{\text{on max}}, \tag{22}$$

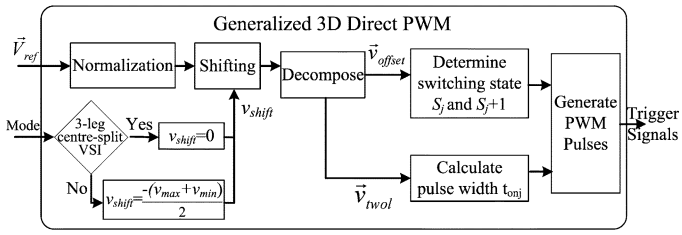


Fig. 5. Flow chart of the generalized 3-D direct PWM.

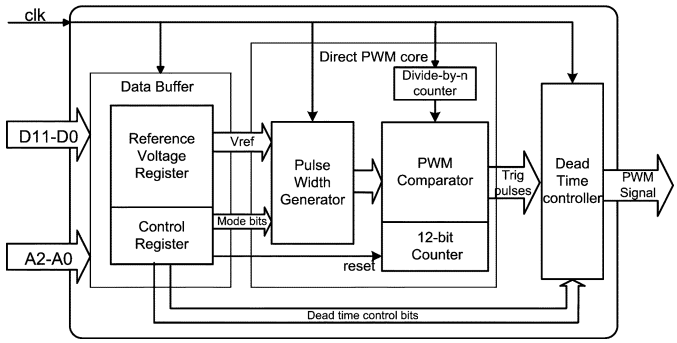


Fig. 6. Block diagram of the generalized PW modulator.

where $t_{\text{on min}}$ is the dwell time of switching states (1,1,1,1), which is also the minimum PW among the four legs, as illustrated in Fig. 5; $1-t_{\text{on max}}$ is the dwell time of switching states (0,0,0,0). If (17) is considered, (23) and (24) can be obtained. Equation (25) is obtained by substituting (23) and (24) into (22)

$$t_{\text{on min}} = v_{\min} + v_{\text{reff}} + 1/2 \tag{23}$$

$$t_{\text{on max}} = v_{\max} + v_{\text{reff}} + 1/2 \tag{24}$$

$$v_{\text{reff}} = -(v_{\max} + v_{\min})/2. \tag{25}$$

Therefore, the shifting voltage is defined as

$$v_{\text{shift}} = -(v_{\max} + v_{\min})/2 \tag{26}$$

where $V_{\max}$ is the maximum number from among v_{af}, v_{bf}, v_{cf} and v_{ff}; is the minimum number from among v_{af}, v_{bf}, v_{cf} and v_{ff}.

C. Modifying 3-D Direct PWM for Four-Leg VSIs

The reference voltage of each leg of a two-level four-leg VSI can be calculated once the shifting voltage has been determined

$$v_{\text{refj}} = v_{jf} + v_{\text{shift}} \quad j = a, b, c, f. \tag{27}$$

According to (17), the output pulses can be generated using the PWs determined by (28) for a two-level four-leg VSI

$$t_{\text{onj}} = v_{jf} + v_{\text{shift}} + 1/2 \quad j = a, b, c, f. \tag{28}$$

For a multilevel four-leg voltage source inverter, (28) is replaced by (29), since the normalized voltage of the mid-point of the dc bus is $(N-1)/2$

$$v_{\text{refj}} = v_{jf} + v_{\text{shift}} + \frac{(N-1)}{2} \quad j = a, b, c, f. \tag{29}$$

If the normalized reference voltage of the fourth-leg of a three-level VSI is 1.4, the switching states of the fourth-leg vary between $S_f = 1$ and $S_f = 2$ in one period, and the dwell time of $S_f = 2$ equals 0.4* T_s. In the 3-D direct PWM, the integer part of v_{refj} determines the switching states of the corresponding leg in one PWM period; the fractional part of v_{refj} determines the PW. Therefore, the 3-D direct PWM is likewise able to control multilevel four-leg VSIs.

IV. Generalized PW Modulator

3-D direct PWM can be applied to three-leg center-split VSIs and four-leg VSIs from two-level to multilevel topologies. Therefore, a generalized 3-D direct PWM is proposed and the flow chart for implementing the generalized 3-D direct PWM is shown in Fig. 5. Since the generalized 3-D direct PWM is based on voltage-second approximation as the conventional SVM, it also has the merits, such as a constant switching frequency, low output ripples, etc.

Based on the 3-D direct PWM, a generalized PW modulator is developed in this paper by using a XILINX XC3S400 FPGA. The FPGA provides benefits, such as high operating frequency, parallel processing capabilities and user definable I/O ports. The design of the generalized PW modulator was described via VHSIC Hardware Description Language (VHDL). The synthesis, placement and route were implemented in an ISE7.1i environment. The frequency of the external clock was 40 MHz, and 19% slices of the FPGA were used. The idle capacity of the FPGA could be used to implement other tasks, such as soft-switching, protection circuits etc. The block diagram of the generalized PW modulator is shown in Fig. 6, which consists of three modules.

A. Data Buffer

The I/O port of the PW modulator consists of a 12-b data bus and a 3-b address bus. The phase-to-neutral reference voltages are modified according to (30), before being transferred to the FPGA in every sampling period

$$\vec{v}_{\text{ref}} = \text{INT}\left[500 \times \begin{bmatrix} V_{\text{refa}}/E \\ V_{\text{refb}}/E \\ V_{\text{refc}}/E \end{bmatrix}\right] + 250(N-1) \tag{30}$$

where N is the level of the VSI and E is the dc voltage of one level. The floating-point arithmetic becomes fixed-point arithmetic via (30).

The period of the digital counter is set to 1000 and its control clock period is 0.2 μs, when the switching frequency is 5 kHz. The period of the control clock is much shorter than the turn-off time of most power switches. For example, the maximum turn-off time of the IGBT used in prototypes is 3 μs. Hence, representing the PWs by an unsigned integer is acceptable when the PW modulator is designed. In addition, 10-b A/D converters are used in prototypes in this paper. When a five-level VSI is controlled, the reference signal sending to the FPGA is in the range of 0–2000. Hence, 12-b integer realization was selected for the design of the PW modulator.

The data buffer also contains a 12-b control register which needs to be initialized before the PW modulator is triggered to operate. The detailed description of the control bits are provided

TABLE I
SWITCHING TABLE OF A THREE-LEVEL VSI

Voltage	S_j	S_{j1}	S_{j2}	S_{j3}	S_{j4}
0	0	Turn-off	Turn-on	Turn-off	Turn-on
E	1	Turn-on	Turn-off	Turn-off	Turn-on
2E	2	Turn-on	Turn-off	Turn-on	Turn-off

hereinafter, in which Bit 0 represents the least significant bit and Bit 11 is the most significant bit.

- Bit 0-1 Level: The level of the inverters to be controlled

Bit 1	Bit 0	Inverter Level *N*
0	0	2
0	1	3
1	0	4
1	1	5

- Bit 2-4 SPD: Input clock prescaler for the PWM core

000	F/2	100	F /32
001	F /4	101	F /64
010	F /8	110	F /128
011	F /16	111	F /256

F= FPGA input clock frequency

- Bit 5 Mode: The topology of the inverter
  - 0 Three-leg center-split VSI.
  - 1 Four-leg VSI.
- Bit 6 Reset: Reset the PWM core
  - 0 Reset entire PWM core(counter is set back to 0).
  - 1 No effect.
- Bit 7 Handshaking
  - 0 The reference data in registers are ready.
  - 1 The reference data in registers are being modified.
- Bit 8-10 SDP: Input clock prescaler for the dead-time controller. Scaling table is the same as that for SPD.
- Bit 11 Reserved.

B. Direct PWM Core

The direct PWM core contains a divide-by-n counter which scales the external input clock to provide clock signals for comparators and 12-b counters. The 12-b up-down counter is triggered by the rising-edge of the "Reset" bit in the control register. The counter first operates in up-counting mode, counting from 0 to 500. The counter is then in down-counting mode until its output reaches 0. The final PWM output frequency can be determined by

$$f = F/r_c/1000 \tag{31}$$

where F is the frequency of the external clock and r_c is the scaling ratio of the divide-by-n counter which is determined by the value of SPD in the control register.

The PW generator calculates the PW of each switch according to the states of control bits "Level" and "Mode." The detailed steps are as follows.

1) The reference signals are read from the registers and the reference voltages of each leg are calculated according to (32), where V_{reff} always equals 250 $(N-1)$

$$V_j = V_{\text{refj}} + V_{\text{shift}} - 250 \times (N-1) \quad j = a, b, c, f \tag{32}$$

where

$$V_{\text{shift}} = \begin{cases} 500 \times (N-1) - \frac{V_{\max}+V_{\min}}{2} & \text{Mode} = 1 \\ 0 & \text{Mode} = 0 \end{cases}. \tag{33}$$

2) Calculate the PW of each switch of the inverter.

In the proposed 3-D direct PWM, the output pulses of each leg are generated as depicted in Figs. 3 and 4. However, the objective of the PW modulator is to generate the trigger signals for every switch of a VSI. The output pulse of each leg in Fig. 3 needs to be transferred to the trigger signals of each switch of a VSI. Conventional SVM solves this problem by means of a switching table. The switching table for a three-level VSI is shown in Table I in which the states of all switches of a leg corresponding to an output voltage are listed.

As the level of the inverter increases, the switching table becomes more complicated and takes up more memory space. A new method is proposed in this paper for the design of the generalized PW modulator in which the PW of each switch is directly determined by the reference voltages. For an N -level VSI there are $2(N-1)$ switches in each leg. The $2(N-1)$ switches are numbered according to the following rule: All the switches above the point where the output voltage is connected are numbered by odd values from $S_{j1}, S_{j3} \cdots$ to $S_{j(2N-3)}$, while all the switches below that point are numbered by even values from $S_{j(2N-2)}, S_{j(2N-4)} \cdots$ to $S_{j2} (j = a, b, c, f)$. The numbering of the switches is illustrated in Fig. 1.

Therefore, the $2(N-1)$ switches of one leg can be divided into $(N-1)$ pairs. If the switch pairs are numbered by odd value 'n' $(0 \le n \le 2N-3)$, the mth pair consists of two switches, which are S_{jm} and $S_{j(m+1)}$. The states of the two switches of the same pair are always opposed. Hence, if the trigger signal for the switch S_{jm} is determined, the trigger signal for its counterpart $S_{j(m+1)}$ can be generated by reversing S_{jm}.

After the switching table was analyzed, it was found that the states of all the odd-numbered switches could be determined according to the value of the switching function S_j. It is assumed that S_j equals K. All the odd-numbered switches whose number is larger than $(2K-1)$ are turned off, and all the odd-numbered switches whose number is less than or equal to $(2K-1)$ are turned on. In the 3-D direct PWM, the output switching state of each leg varies between S_j and $S_j + 1$ during one PWM period. Hence, the switches from S_{j1} to $S_{j(2K-1)}$ are turned on during the whole period. Switches whose numbers are larger than $(2K+1)$, are always turned off. Switch $S_{j(2K+1)}$ is first turned off, and then turned on when the output state is changed to $S_j + 1$. The PW of $S_j + 1$ is simply the PW of the trigger signal of switch $S_{j(2K+1)}$. Therefore, the PW of each switch can be determined by

$$\begin{aligned} T_{jn} &= 250(N-m) + (V_{jn} - 250(N-1)) \\ &= 250(1-m) + V_{jn} \quad j = a, b, c, f. \end{aligned} \tag{34}$$

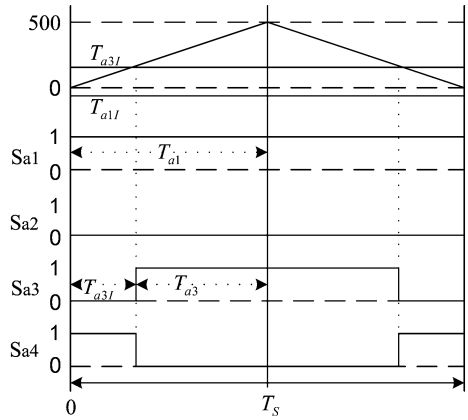


Fig. 7. Generation the trigger signals for a three-level VSI.

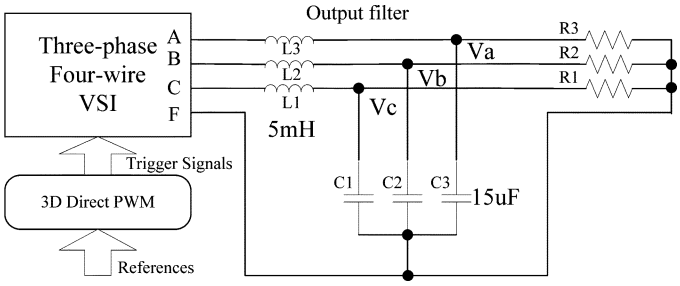


Fig. 8. Simulation system configuration.

If the symmetrical aligned scheme is adopted in generating the trigger signals, the value, which is compared against the output of the counter, is expressed as

$$T_{\text{jnI}} = (500 - T_{jn})/2 = 250(m+1) - V_{jn} \quad j = a, b, c, f. \tag{35}$$

The T_{jnI} is compared to the output of the 12-b counter at every falling edge of the clock signal. When the output of the counter is larger than the T_{jnI} of the mth switch, the trigger signal of this switch is forced into high mode. Otherwise, the trigger signal is low. The switching state of the switch with the number $m+1$ is obtained by reversing that of the mth switch. Generation of the trigger signals of the four switches of leg A of a three-level inverter is illustrated in Fig. 7.

In this case, T_{a3I} and T_{a1I} are calculated by (35) and compared to the output of the counter to determine trigger signals of the switches S_{a1} and S_{a3}. The trigger signals of switches S_{a2} and S_{a4} are obtained by reversing that of S_{a1} and S_{a3}, respectively.

C. Dead-Time Controller

The dead-time controller is included in the generalized PW modulator so that dead-times fit into the transition edges of the trigger signals. The input clock of the dead-time controller is first scaled according to the control bit "SDP." The corresponding clock that is obtained is used as the clock signal for a counter which periodically counts from "0" to "40." Hence, the dead-time is calculated by

$$T_d = 40/(F/r_d) \tag{36}$$

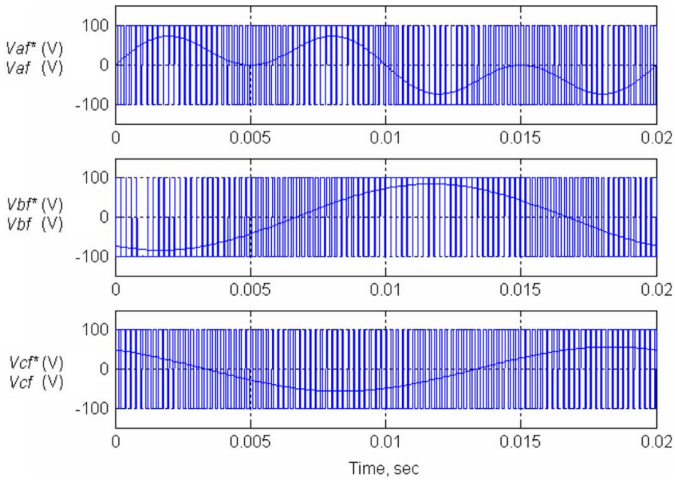


Fig. 9. Output voltage of a two-level three-leg center-split VSI.

where F is the input frequency of the external clock and r_d is the scaling ratio.

V. Simulation Results

Simulations are implemented by Matlab/Simulink. The simulation system configuration is shown in Fig. 8. The output voltages of the inverter are passed through an output filter and applied to three-phase balanced loads. The filter is designed to smooth the pulse train and recovers average analog waveforms. The proposed generalized 3-D direct PWM is applied in order to control the three-phase four-wire VSIs to track reference voltages.

The reference voltages are selected to illustrate that both pure sinusoidal and harmonic-injection phase-to-neutral voltages can be generated by using the proposed 3-D direct PWM. A two-level center-split VSI, a three-level center-split VSI, a five-level center-split VSI, a two-level four-leg VSI and a three-level four-leg VSI are controlled respectively. The reference and output voltages of each leg of the corresponding VSIs are shown in Figs. 9 –13.

The voltages after passing the filter and currents through the loads when a three-level center-split VSI is used are shown in Fig. 14. Similar results were obtained in the four other cases.

The total harmonic distortion (THD) and root mean square (RMS) values of the output voltages after passing the filter are provided in Table II. The simulation results indicate that the generalized 3-D direct PWM can control the three-leg center-split VSI and four-leg VSI from two-level to multilevel topologies.

VI. Experimental Results

A. Testing Generalized PW Modulator

Prototypes for a two-level center-split VSI, a two-level four-leg VSI and a three-level center-split VSI were built. The FPGA-based generalized PW modulator was applied to control these VSIs to track the given references. The block diagram for the control system is shown in Fig. 15. A DSP (TMS320F2407) was used to generate the reference voltages and send the references to the data buffers in FPGA.

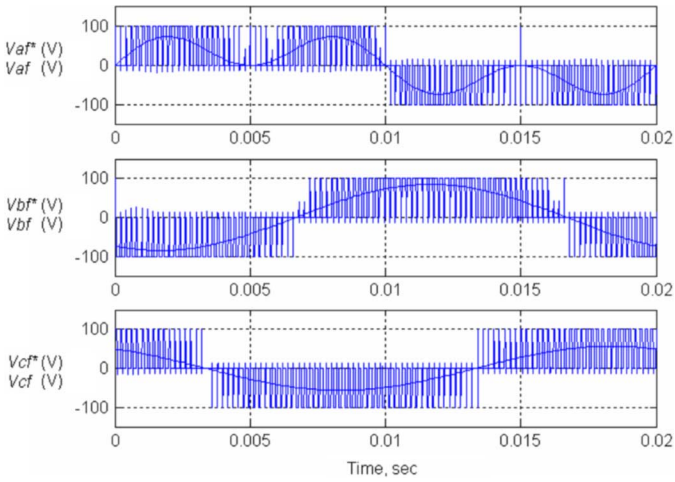


Fig. 10. Output voltage of a three-level three-leg center-split VSI.

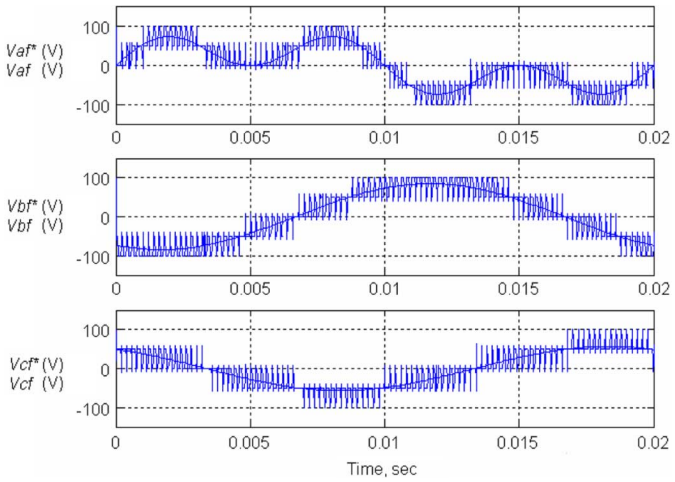


Fig. 11. Output voltage of a five-level three-leg center-split VSI.

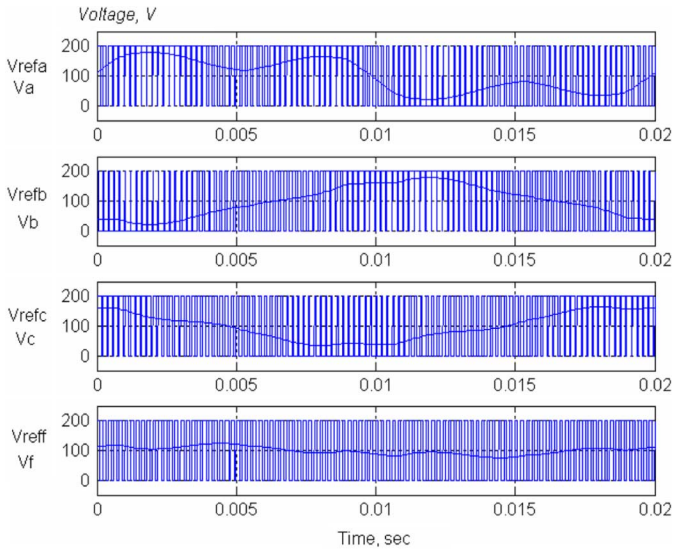


Fig. 12. Output voltage of a two-level four-leg VSI.

The RMS value and THD of the references, which are generated by the 16-b fixed point DSP, are listed in Table III. The dc bus voltage is 200 V and PWM frequency is 5 kHz. The experimental system configuration is the same as that in

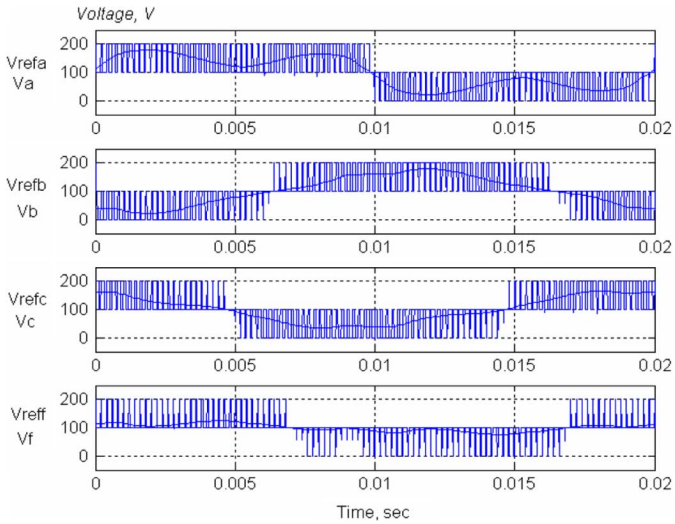


Fig. 13. Output voltage of a three-level four-leg VSI.

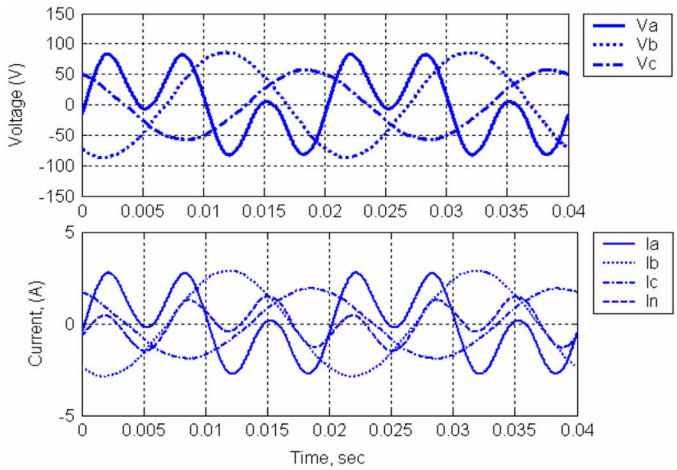


Fig. 14. Voltages across the loads and the currents passing through the loads.

TABLE II
PARAMETERS OF SIMULATION RESULTS

	THD (%)			RMS (V)		
	A	B	C	A	B	C
Reference voltages	100	1.0	1.0	48.08	60	40
Two-level centre-split VSI	105	1.71	2.75	49.58	60.34	40.24
Three-level centre-split VSI	105	1.13	1.70	49.53	60.3	40.18
Five-level centre-split VSI	105	0.67	1.11	48.99	59.86	39.51
Two-level four-leg VSI	104.9	2.37	2.44	49.58	60.33	40.25
Three-level four-leg VSI	103.2	2.0	2.8	49.01	59.74	40.01

simulations. The experimental results of controlling a two-level center-split VSI, a three-level center-split VSI and a two-level four-leg VSI are shown in Figs. 16 –18, in which the output voltages of the VSIs, the voltage across the loads and the current passing through the loads are provided. Neutral currents are also recorded.

The RMS and THD of the voltages across the loads are provided in Table III. The experimental results show that the FPGA-based generalized PW modulator can control the three-phase four-wire VSIs to trace the given references. However, the THD values of the two-level four-leg VSI are not satisfactory. In the experiment, the inserted dead-time affects the performance of

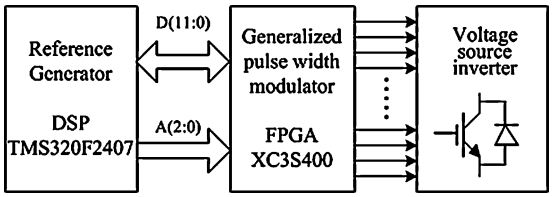


Fig. 15. Block diagram for the control system.

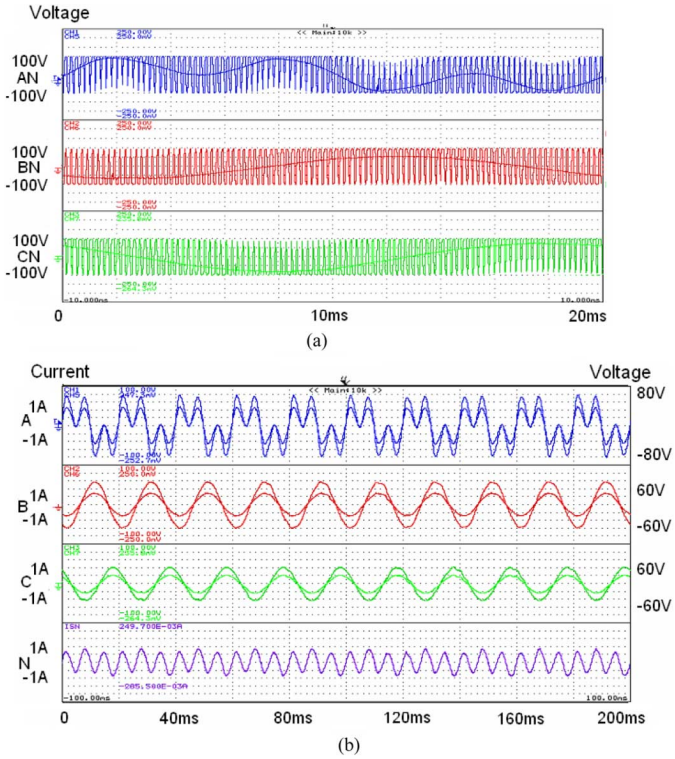


Fig. 16. Experimental results of a two-level center-split VSI: (a) output voltages of the VSI and (b) load voltages and currents.

the four-leg VSI. The performance of the two-level four-leg VSI is deteriorated when the reference voltage of the fourth-leg is low compared to the dc bus voltage. Better performance can be obtained when the modulation index is increased.

B. Applications of Generalized PW Modulator in Three-Phase Four-Wire APFs

Three-phase four-wire active power filter prototypes were also built, as shown in Fig. 19, in which a two-level four-leg VSI and a three-level center-split VSI are used, respectively. The control system configuration is the same as that in Fig. 15.

The DSP is used to calculate the reference voltages. The instantaneous reference current, for the sake of compensation, is determined by the generalized instantaneous reactive power theory [16]. The reference voltage vector at time KT is calculated by (37), [19], where T is the fixed sampling period

$$\begin{aligned}\vec{v}[\mathrm{KT}] = \vec{v}_S[\mathrm{KT}] \\ - \frac{R_c}{\Delta X}\{\vec{i}_c^{\,*}[\mathrm{KT}] \\ - (1-\Delta X)\vec{i}_c[\mathrm{KT}]\}\end{aligned} \tag{37}$$

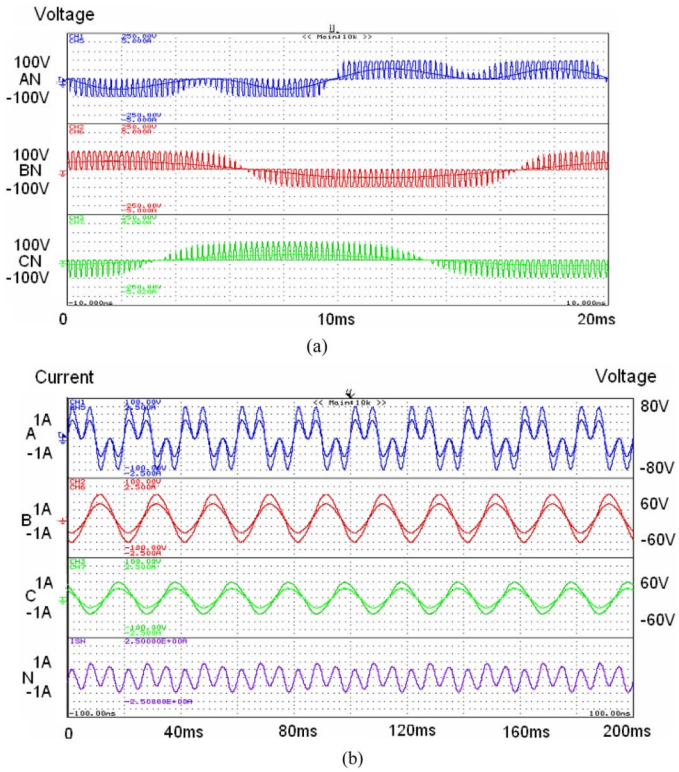


Fig. 17. Experimental results of a three-level center-split VSI: (a) output voltages of the VSI and (b) load voltages and currents.

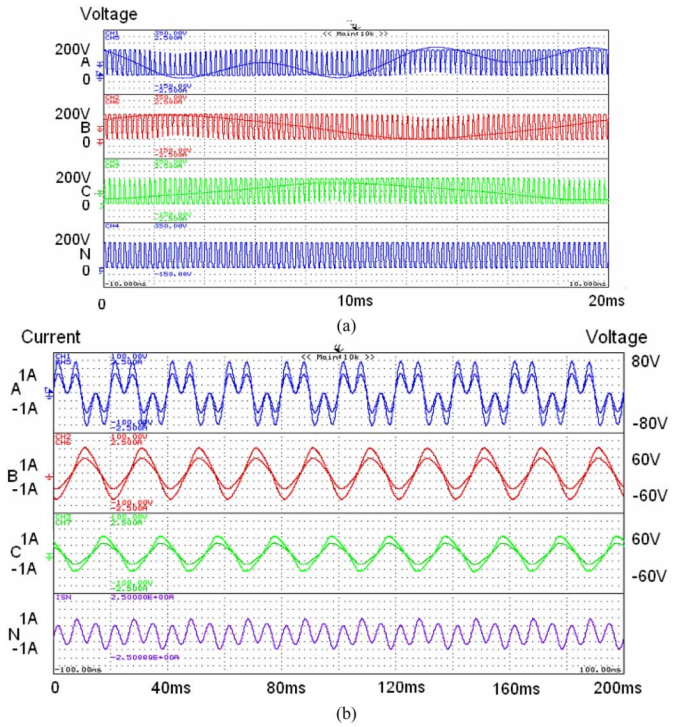


Fig. 18. Experimental results of a two-level four-leg VSI: (a) output voltages of the VSI and (b) load voltages and currents.

where

$$\Delta X = \frac{R_c}{L_c} \cdot e^{-\frac{R_c}{L_c}T} \cdot T.$$

TABLE III
PARAMETERS OF EXPERIMENTAL RESULTS

	THD (%)			RMS (V)		
	A	B	C	A	B	C
References	100	1.7	1.7	50	44.1	35.35
Two-level centre-split VSI	104.8	3.1	2.1	48.6	41.06	29.36
Three-level centre-split VSI	104.8	2.5	3.3	50.2	41.76	27.50
Two-level four-leg VSI	102.8	4.8	6.8	50.2	43.2	28.75

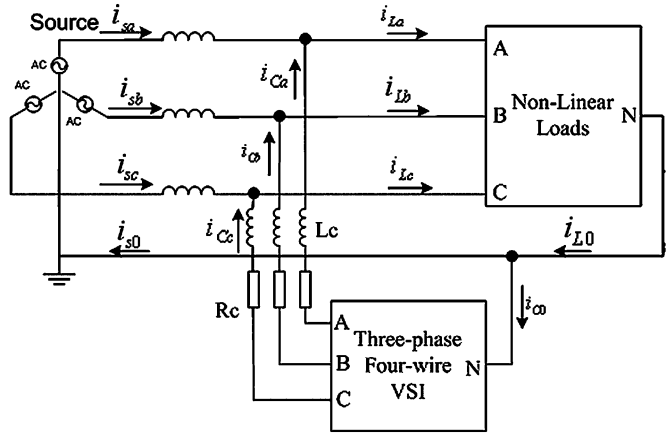


Fig. 19. System configuration of a three-phase four-wire APF.

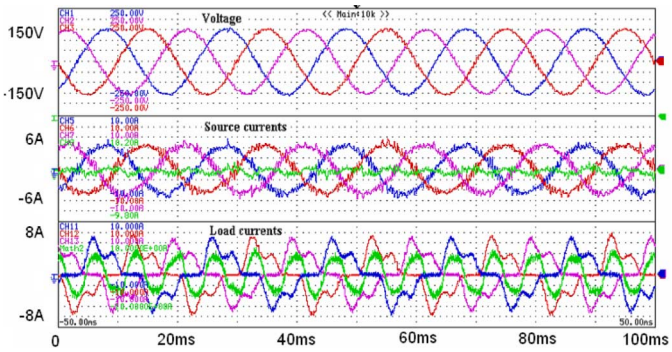


Fig. 20. Current compensation of the APF using a two-level four-leg VSI.

The generalized PW modulator controls three-level center-split VSIs to track the obtained references, compensating for the current problems experienced in quality. When a two-level four-leg voltage source inverter is used, the neutral wire is connected to the fourth-leg of the voltage source inverter. The system voltage, load currents and source currents after compensation are shown in Fig. 20.

The THD of the load currents is approximately 30.2%. In the experiment, the non-linear loads are connected to a 10 kVA isolation transformer. The fundamental frequency component of the maximum demand current of the loads are 5 A, and the maximum short-circuit current at the point of common coupling (PCC) is about 300 A. The THD after compensation should be less than 12% according to the Std. IEEE 519:1992 recommendation [31]. The THD of the source currents after compensation is reduced to 7.1%. The neutral current is also greatly reduced after compensation.

When a three-level center-split VSI is used in the three-phase four-wire APF, the load currents and the source currents after compensation are shown in Figs. 21 and 22, respectively. The corresponding THD values are listed in Table IV, in which the RMS values of the neutral current before and after compensation are also shown.

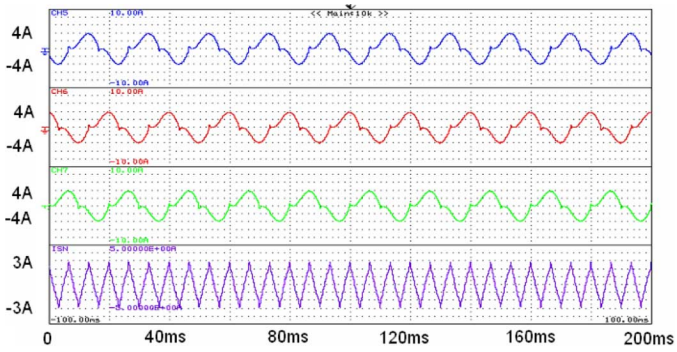


Fig. 21. Load Currents.

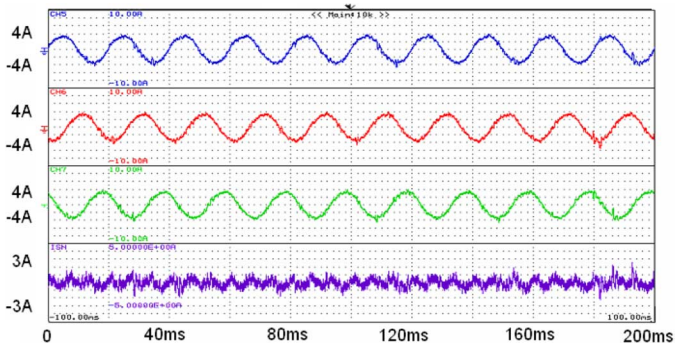
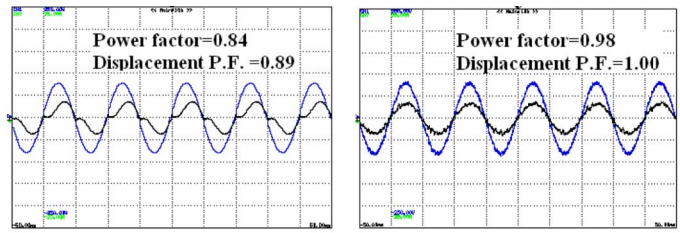


Fig. 22. Source current after compensation by using a three-level center-split VSI.

TABLE IV
COMPENSATION RESULTS OF APF

	THD A	THD B	THD C	Neutral
Load currents	25.2%	25.3%	25.4%	1.56A
Source currents after compensation	7.5%	6.5%	6.2%	0.53A



(a) (b)

Fig. 23. Reactive power compensation (a) voltage and load current and (b) voltage and source current.

Reactive power compensation is illustrated in Fig. 23, where Fig. 23(a) shows the system voltage and load current and Fig. 23(b) shows the system voltage and source current after compensation. The corresponding power factor and displacement power factor are provided in Fig. 23. The results indicate that the current harmonics, reactive currents and neutral current are compensated simultaneously by using the proposed generalized PW modulator to control the APF.

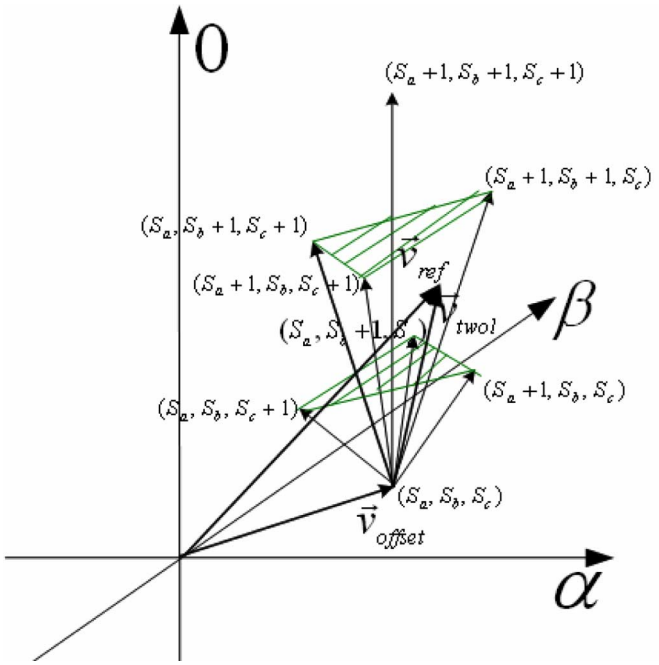


Fig. 24. Space vector allocation for two-level vectors in the $\alpha - \beta{-}0$ coordinates.

VII. Conclusion

In this paper, a generalized 3-D direct PWM is proposed which can control the two most widely used three-phase four-wire VSIs—three-leg center-split VSIs and four-leg VSIs—from two-level to multilevel topologies. The proposed 3-D direct PWM is based on voltage-second approximation and generates PWM outputs according to the reference of each leg. A shifting voltage is introduced in order to determine the reference of each leg of a four-leg VSI. In this way the 3-D direct PWM is likewise able to control four-leg VSIs. Simulation results are provided to show the validity of the generalized 3-D direct PWM.

In order to release the loads of the digital controllers and save the time for implementing PWM for each specific inverter, a FPGA-based generalized PW modulator was developed according to the 3-D direct PWM outlined in this paper. The generalized PW modulator is able to control three-leg center-split VSIs and four-leg VSIs from two-level to multilevel topologies. Experimental results are provided to show that the generalized PW modulator can control the three-phase four-wire VSIs to track the reference voltages.

Therefore, the proposed generalized PW modulator can be used in applications such as adjustable speed drivers and uninterruptible power supplies, where three-phase balanced reference voltages are adopted. It can also be applied in cases where unbalanced and harmonic-injection references are used, such as active power filters and dynamic voltage restorers. In this paper, the generalized PW modulator is applied to active power filters to control three-phase four-wire VSIs. The experimental results indicate that the current harmonics, reactive currents, and neutral current can be compensated simultaneously by the proposed PW modulator.

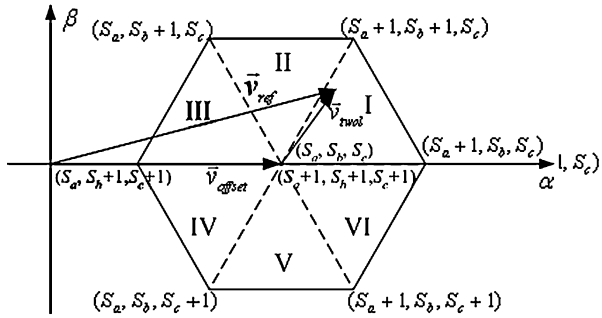


Fig. 25. Projection of Space vector allocation for two-level vectors on the $\alpha - \beta$ plane.

Appendix

In this section, the equivalence between the 3-D direct PWM and 3-D SVM in [15] is proved when a multilevel three-leg center-split VSI is controlled. The normalized reference voltage vector is decomposed into an offset voltage vector and a two-level voltage vector in the 3-D SVM

$$\vec{v}_{\text{ref}} = \vec{v}_{\text{offset}} + \vec{v}_{\text{twol}} \tag{A1}$$

where

$$\vec{v}_{\text{offset}} = \begin{bmatrix} v_{\text{offseta}} \\ v_{\text{offsetb}} \\ v_{\text{offsetc}} \end{bmatrix} = \begin{bmatrix} \text{Int}(v_{\text{refa}}) \\ \text{Int}(v_{\text{refb}}) \\ \text{Int}(v_{\text{refc}}) \end{bmatrix}. \tag{A2}$$

If $(v_{\text{offseta}}, v_{\text{offsetb}}, v_{\text{offsetc}})$ equals (Sa, Sb, Sc), the reference voltage vector must be located within the confines of a two-level space vector allocation as shown in Fig. 24 in the $\alpha - \beta{-}0$ coordinates. The projection on the $\alpha - \beta$ plane is shown in Fig. 25.

In the 3-D SVM, the reference voltage vector is synthesized by four neighbouring vectors. If the dwell time of each vector is normalized by the PWM period T_s, (A3) and (A4) can be obtained

$$\vec{v}_{\text{ref}} = \vec{v}_1 t_1 + \vec{v}_2 t_2 + \vec{v}_3 t_3 + \vec{v}_4 t_4 \tag{A3}$$

$$t_1 + t_2 + t_3 + t_4 = 1. \tag{A4}$$

The neighbouring vector $\vec{v}_1$ is the offset vector determined by (A2), which is located at the center point of the eight vectors on the $\alpha - \beta$ plane. $\vec{v}_2$ and $\vec{v}_3$ are the neighbouring vectors of the reference voltage vector on the $\alpha - \beta$ plane. The zero-sequence compensation is achieved by introducing the fourth vector in reference voltage approximation, and is always $(S_a + 1, S_b + 1, S_c + 1)$. Hence, each section on the $\alpha - \beta$ plane, as illustrated in Fig. 25, corresponds to one output switching sequence. The switching sequences and boundary conditions for each section are provided in Table V. The dwell times are also provided in Table V. After the dwell times of each neighbouring vector are determined, the PW output can be generated, also illustrated in Fig. 3.

The two-level voltage vector can be expressed in the a-b-c coordinates as (A5). According to the $\alpha - \beta{-}0$ transformation,

TABLE V
BOUNDARY CONDITIONS, NEIGHBOURING VECTORS AND DWELL TIMES OF 3-D SVM

Section	Boundary conditions	Neighboring Vectors	Dwell times
I	$v_{twol\beta} > 0$ $v_{twol\alpha} > 0$ $v_{twol\beta} - \sqrt{3}v_{twol\alpha} < 0$	$\vec{v}_1 = (S_a, S_b, S_c)$ $\vec{v}_2 = (S_a+1, S_b, S_c)$ $\vec{v}_3 = (S_a+1, S_b+1, S_c)$ $\vec{v}_4 = (S_a+1, S_b+1, S_c+1)$	$t_1 = 1 - t_2 - t_3 - t_4$ $t_2 = (\sqrt{3}/2)v_{twol\alpha} - 0.5t_3$ $t_3 = \sqrt{2}v_{twol\beta}$ $t_4 = v_{twol0}/\sqrt{3} - t_2/3 - 2t_3/3$
II	$v_{twol\beta} > 0$ $\lvert v_{twol\beta}\rvert - \sqrt{3}\lvert v_{twol\alpha}\rvert > 0$	$\vec{v}_1 = (S_a, S_b, S_c)$ $\vec{v}_2 = (S_a, S_b+1, S_c)$ $\vec{v}_3 = (S_a+1, S_b+1, S_c)$ $\vec{v}_4 = (S_a+1, S_b+1, S_c+1)$	$t_1 = 1 - t_2 - t_3 - t_4$ $t_2 = t_3 - \sqrt{6}v_{twol\alpha}$ $t_3 = \sqrt{3/2}v_{twol\alpha} + \sqrt{1/2}v_{twol\beta}$ $t_4 = v_{twol0}/\sqrt{3} - t_2/3 - 2t_3/3$
III	$v_{twol\beta} > 0$ $v_{twol\alpha} < 0$ $v_{twol\beta} + \sqrt{3}v_{twol\alpha} < 0$	$\vec{v}_1 = (S_a, S_b, S_c)$ $\vec{v}_2 = (S_a, S_b+1, S_c)$ $\vec{v}_3 = (S_a, S_b+1, S_c+1)$ $\vec{v}_4 = (S_a+1, S_b+1, S_c+1)$	$t_1 = 1 - t_2 - t_3 - t_4$ $t_2 = \sqrt{2}v_{twol\beta}$ $t_3 = (-\sqrt{3}/2)v_{twol\alpha} - 0.5 \cdot t_2$ $t_4 = v_{twol0}/\sqrt{3} - t_2/3 - 2t_3/3$
IV	$v_{twol\beta} < 0$ $v_{twol\alpha} < 0$ $v_{twol\beta} - \sqrt{3}v_{twol\alpha} > 0$	$\vec{v}_1 = (S_a, S_b, S_c)$ $\vec{v}_2 = (S_a, S_b, S_c+1)$ $\vec{v}_3 = (S_a, S_b+1, S_c+1)$ $\vec{v}_4 = (S_a+1, S_b+1, S_c+1)$	$t_1 = 1 - t_2 - t_3 - t_4$ $t_2 = -\sqrt{2}v_{twol\beta}$ $t_3 = (-\sqrt{3}/2)v_{twol\alpha} - 0.5 \cdot t_2$ $t_4 = v_{twol0}/\sqrt{3} - t_2/3 - 2t_3/3$
V	$v_{twol\beta} < 0$ $\lvert v_{twol\beta}\rvert - \sqrt{3}\lvert v_{twol\alpha}\rvert > 0$	$\vec{v}_1 = (S_a, S_b, S_c)$ $\vec{v}_2 = (S_a, S_b, S_c+1)$ $\vec{v}_3 = (S_a+1, S_b, S_c+1)$ $\vec{v}_4 = (S_a+1, S_b+1, S_c+1)$	$t_1 = 1 - t_2 - t_3 - t_4$ $t_2 = t_3 - \sqrt{6}v_{twol\alpha}$ $t_3 = \sqrt{3/2}v_{twol\alpha} - \sqrt{1/2}v_{twol\beta}$ $t_4 = v_{twol0}/\sqrt{3} - t_2/3 - 2t_3/3$
VI	$v_{twol\beta} < 0$ $v_{twol\alpha} > 0$ $v_{twol\beta} + \sqrt{3}v_{twol\alpha} > 0$	$\vec{v}_1 = (S_a, S_b, S_c)$ $\vec{v}_2 = (S_a+1, S_b, S_c)$ $\vec{v}_3 = (S_a+1, S_b, S_c+1)$ $\vec{v}_4 = (S_a+1, S_b+1, S_c+1)$	$t_1 = 1 - t_2 - t_3 - t_4$ $t_2 = (\sqrt{3}/2)v_{twol\alpha} - 0.5 \cdot t_3$ $t_3 = -\sqrt{2}v_{twol\beta}$ $t_4 = v_{twol0}/\sqrt{3} - t_2/3 - 2t_3/3$

the two-level voltage vector in the $\alpha - \beta - 0$ coordinates can be expressed as (A6).

$$\vec{v}_{\text{ref}} = v_{\text{twola}}\vec{n}_a + v_{\text{twolb}}\vec{n}_b + v_{\text{twoc}}\vec{n}_c \tag{A5}$$

$$\begin{cases} v_{\text{twol}\alpha} = \sqrt{\frac{2}{3}}\left(v_{\text{twola}} - \frac{1}{2}v_{\text{twolb}} - \frac{1}{2}v_{\text{twolc}}\right) \\ v_{\text{twol}\beta} = \frac{1}{\sqrt{2}}(v_{\text{twolb}} - v_{\text{twolc}}) \\ v_{\text{twol0}} = \frac{1}{\sqrt{3}}(v_{\text{twola}} + v_{\text{twolb}} + v_{\text{twolc}}) \end{cases} \tag{A6}$$

If the sequence in Fig. 3 is chosen as an example, the PW of each phase are expressed as

$$\begin{cases} t_{\text{ona}} = t_2 + t_3 + t_4 \\ t_{\text{onb}} = t_3 + t_4 \\ t_{\text{onc}} = t_4 \end{cases} \tag{A7}$$

where $t_{\text{ona}}, t_{\text{onb}}$ and t_{onc} are the PWs, as shown in Fig. 3. The sequencing in Fig. 3 corresponds to the Section I in Table V. If the formula for calculating dwell times in Table V and (A6) are substituted to (A7), (A8) can be obtained

$$t_{\text{onj}} = v_{\text{twolj}} \quad j = a, b, c. \tag{A8}$$

Equation (A8) indicates that the PW of each phase equals the normalized two-level reference voltages. It can be proved that (A8) is also valid if the reference voltage vector is located in the other five sections. Equation (A8) is the same as (13) which is used for calculating the PW of each leg in the 3-D direct PWM. Therefore, the equivalence between 3-D direct PWM and the 3-D SVM is proved.

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