Application of 3D Direct PWM in Parallel Power Quality Compensators in Three-phase Four-wire Systems

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Abstract—**The 3D direct pulse width modulation (PWM) for three-leg centre-split voltage source inverters (VSIs) and four-leg VSIs is proposed in this paper. It can be applied to these VSIs from two-level to multi-level systems. The generalized 3D direct PWM implements the voltage synthesis in per-leg mode and it is based on the voltage second approximation as the conventional space vector modulation (SVM). As a result, it also has the merits of conventional SVM, such as a constant switching frequency, low output ripples, etc. However, the computational cost of the proposed 3D direct PWM is much lower than the SVM. The proposed 3D direct PWM is applied to control a four-leg inverter in an active power filter and a three-leg centre-split inverter in a hybrid filter in three-phase four-wire systems. Simulation results are provided to show the validities of the proposed 3D direct PWM.**

I. INTRODUCTION

According to the proliferation and development of power electronics equipments in automatic production line, computer centre, hospital, etc; the power quality in three-phase four-wire distribution system is deteriorated. Harmonic distortion may cause equipment overheating, capacitor fuse blowing, etc. In order to eliminate the harmonic currents, active power filters (APF) and hybrid filters are placed between the load and the source side [1]-[3].

Voltage source inverters (VSIs) with a neutral wire connection are important for power quality compensators in three-phase four-wire distribution systems [4]-[8]. Three-phase voltage source inverters have two ways of providing a neutral connection: 1) using split dc-linked capacitors and tying the neutral point to the mid-point of the dc linked capacitors; 2) using a four-leg inverter topology and tying the neutral point to the mid-point of the fourth neutral leg. For medium and large capacity applications, a multi-level three-phase four-wire VSI is a better solution than a two-level one [9]-[11].

The VSIs are controlled by pulse width modulation (PWM) methods to generate the required voltages or currents according to the references. In a three-phase four-wire system, the reference vector is not on the α-β plane if the system is unbalanced, or if there is a zero sequence or triple harmonics [12]. As a result, the PWM methods of three-phase four-wire VSIs are realized in a 3-dimensional (3D) space. The space vector modulation (SVM) is based on voltage-second approximation. It reduces commutation losses and harmonic contents of output voltages, and provides more efficient use of supply voltages in comparison with the hysteresis PWM. The 3D SVM methods of multi-level three-leg centre-split VSIs were proposed [13][14]. The 3D SVM methods of two-level four-leg inverters were also proposed [15][16].

Although much progress has been made, SVM for three-phase four-wire VSIs still involves complex calculations. In addition, implementing PWM for each specific three-phase four-wire VSI in different applications is a time-consuming task for most researchers. If a generalized PWM method is available for controlling the three-phase four-wire VSIs of different topologies and levels, much effort and time could be saved.

In this paper, a generalized 3D direct PWM is proposed, which also based on voltage second approximation as conventional SVM. However, the reference voltages are synthesized in per-leg mode in the proposed 3D direct PWM, and the computational cost is much lower than SVM. The generalized 3D direct PWM can be applied to control three-leg centre-split inverter and four-leg inverter from two-level to multi-level topologies in three-phase four-wire systems.

The proposed 3D direct PWM is applied to control three-phase four-wire parallel power quality compensators in this paper. With the 3D direct PWM, a two-level four-leg VSI of an active power filter and a two-level centre-split VSI of a three-phase four-wire hybrid filter can be controlled respectively. Harmonic components, reactive components of the non-linear load currents together with the neutral currents in a three-phase four-wire system are compensated simultaneously. Simulation results are provided to show the validity of the proposed 3D direct PWM.

II. 3D DIRECT PWM FOR THREE-PHASE FOUR-WIRE VSIS

A. 3D Direct PWM for three-leg centre-split VSI

The 3D direct PWM for three-leg centre-split VSI is first proposed in this section. An equivalent model for an *N*-level three-leg centre-split VSI is shown in Fig. 1.

The output voltage of each leg is expressed as:

$$V_j = E^* S_j \quad j=a,b,c, \tag{1}$$

where E is the voltage of one level, and S_j is the switching function.

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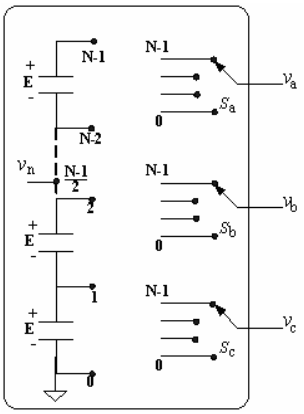

Figure 1. Equivalent model of a three-leg N-level VSI

For an *N*-level inverter, the value of S_j varies among 0 to *N-1*, and the dc bus voltage equals *(N-1)E*. When the *N*-level three-leg centre-split inverters are applied to a three-phase four-wire system, the neutral wire is connected to the mid-point of the dc bus. Hence, the voltage V_n in reference to the virtual ground in Fig. 1 is expressed as:

$$V_n = E*(N-1)/2. \tag{2}$$

All the voltages are expressed per unit, i.e., normalized by *E*, so that the output voltage of each leg has the same value as the switching function S_j.

$$v_j = S_j \qquad j=a,b,c \tag{3}$$

and

$$v_n = (N-1)/2 \tag{4}$$

Normalization facilitates the following steps in the proposed 3D direct PWM. The phase-to-neutral reference voltages are also normalized by *E*, as given in (5). v_n is added to the reference voltages, so that both the output voltages of the inverter and the reference voltages are in reference to the same virtual ground.

$$\vec{v}_{ref} = \vec{V}_{ref}/E + V_n/E = \begin{bmatrix} V_{af}/E \\ V_{bf}/E \\ V_{cf}/E \end{bmatrix} + \frac{N-1}{2} \tag{5}$$

In the 3D direct PWM, the reference voltage vector is first split into two components as (6), which are also expressed in the a-b-c coordinates in (7).

$$\vec{v}_{ref} = \vec{v}_{offset} + \vec{v}_{twol} \tag{6}$$

$$\begin{bmatrix} v_{refa} \\ v_{refb} \\ v_{refc} \end{bmatrix} = \begin{bmatrix} v_{offseta} \\ v_{offsetb} \\ v_{offsetc} \end{bmatrix} + \begin{bmatrix} v_{twola} \\ v_{twolb} \\ v_{twolc} \end{bmatrix} \tag{7}$$

The offset component of the reference voltage is defined as:

$$\vec{v}_{offset} = \begin{bmatrix} v_{offseta} \\ v_{offsetb} \\ v_{offsetc} \end{bmatrix} = \begin{bmatrix} Int(v_{refa}) \\ Int(v_{refb}) \\ Int(v_{refc}) \end{bmatrix}, \tag{8}$$

where *Int*( ) removes the fractional part of the real input data. Consequently, the two-level component of the reference voltage is the fractional part.

$$\vec{v}_{twol} = \vec{v}_{ref} - \vec{v}_{offset} = \begin{bmatrix} v_{twola} \\ v_{twolb} \\ v_{twolc} \end{bmatrix} \tag{9}$$

where $0 \le v_{twol(j)} < 1$ (*j=a,b,c*).

If $(v_{offseta}, v_{offsetb}, v_{offsetc})$ equals (S_a, S_b, S_c), the reference voltage vector must be located inside a two-level space vector allocation formed by vectors: (S_a, S_b, S_c), (S_a+1, S_b, S_c), (S_a, S_b+1, S_c), (S_a, S_b, S_c+1), (S_a+1, S_b+1, S_c), (S_a+1, S_b, S_c+1), (S_a, S_b+1, S_c+1) and (S_a+1, S_b+1, S_c+1).

The proposed 3D direct PWM is based on the voltage-second approximation as the conventional space vector modulation. In order to reduce the switching losses and the output ripples, the output voltage of each leg changes only one level in one period. Therefore, determining the dwell times of the two switching states $v_{offsetj}$ and $v_{offsetj}+1$ can generate the PWM outputs in every period. The dwell time of $v_{offsetj}+1$ (*j=a,b,c*) is calculated by voltage-second approximation in per-phase mode, i.e., the reference voltage is synthesized in phases A, B and C independently.

$$v_{refj} \cdot 1 = v_{offsetj} \cdot t_{offj} + (v_{offsetj} + 1) \cdot t_{onj} \qquad j=a,b,c \tag{10}$$

$$t_{offj} + t_{onj} = 1 \qquad j=a,b,c \tag{11}$$

The t_{offj} is the dwell time of the output state $\boldsymbol{v}_{offsetj}$, and t_{onj} is the dwell time of $\boldsymbol{v}_{offsetj}+1$. Both t_{offj} and t_{onj} are already normalized by T_s which is the period for generating PWM outputs. Eq. (12) is obtained by subtracting $\boldsymbol{v}_{offsetj}$ from both sides of (10).

$$\begin{aligned} v_{refj} - v_{offsetj} &= v_{offsetj} t_{offj} + (v_{offsetj} + 1) t_{onj} \\ &\quad - v_{offsetj}(t_{offj} + t_{onj}) = t_{onj} \end{aligned} \tag{12}$$

Since $v_{refj} - v_{offsetj} = v_{twolj}$ (*j=a,b,c*), it can be concluded that:

$$t_{onj} = v_{twolj} \qquad j=a,b,c \tag{13}$$

and

$$t_{offj} = 1 - v_{twolj} \qquad j=a,b,c \tag{14}$$

Equation (13) indicates that the normalized two-level reference voltage is equal to the normalized pulse width of the corresponding phase. According to the switching states and pulse width, the switching patterns are determined as illustrated in Fig. 2.The final trigger signals of each switch of one inverter leg are then generated.

B. 3D Direct PWM for four-leg VSI

The 3D direct PWM could also be extended to control four-leg VSIs. The topology of a three-level four-leg VSI is shown in Fig.3.

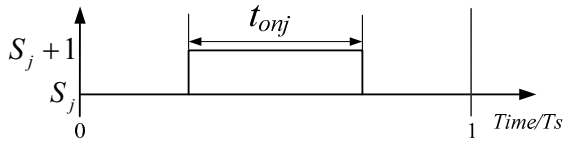

Figure 2. Output pulse width of one leg

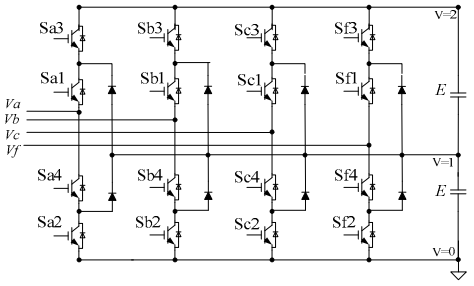

Figure 3. Output pulse width of one leg

For a multi-level four-leg voltage source inverter, the PWM output of each leg is determined in the same way if the reference voltage of each leg is known.

The v_{jf} (j=a,b,c) is the phase-to-neutral reference voltage for controlling three-phase four-wire VSIs, which are also used in (5). The v_{ff} is defined for the fourth leg of a four-leg VSI. The v_{ff} should always equal zero since the system neutral is connected to the output of the fourth-leg.

The output phase-to-neutral voltages of two-level four-leg VSIs are determined by the difference between the output voltages of leg j (j=a,b,c) and the fourth-leg f. The reference output voltage of each leg of a four-leg VSI is calculated by (15) [10]. According to (15), the output voltages of the four-leg inverter equal the phase-to-neutral reference, as illustrated in (16).

$$v_{refj} = v_{jf} + v_{shift} + \frac{(N-1)}{2} \qquad j=a,b,c,f \tag{15}$$

$$v_{refj} - v_{reff} = v_{jf} \quad j=a,b,c \tag{16}$$

The shifting voltage is defined as (17), so that the optimal switching sequence can be achieved.

$$v_{shift} = -(v_{\max} + v_{\min})/2, \tag{17}$$

where $v_{\max}$ is the maximum number from among v_{af}, v_{bf}, v_{cf} and v_{ff}; $v_{\min}$ is the minimum number from among v_{af}, v_{bf}, v_{cf} and v_{ff}.

According to (6) and (13), the output pulses of legs A, B, C and F of a four-leg VSI can be generated. The output pulses of a two-level four-leg VSI are shown in Fig.4. There are redundant times in one PWM period which are taken up by the switching states (0,0,0,0) and (1,1,1,1). The output phase-to-neutral voltages are zero when the four-leg VSI operates according to the two switching patterns. When the shifting voltage is defined as (17), the dwell times of states (0,0,0,0) and (1,1,1,1) are the same and the optimal switching sequence is achieved as expressed in (18).

$$t_{on\,min} = 1 - t_{on\,max,} \tag{18}$$

where $t_{on\,min}$ represents the dwell time of switching states (1,1,1,1). It is also the minimum pulse width among the f our legs. 1- $t_{on\,max}$ is the dwell time of switching states (0, 0,0,0).

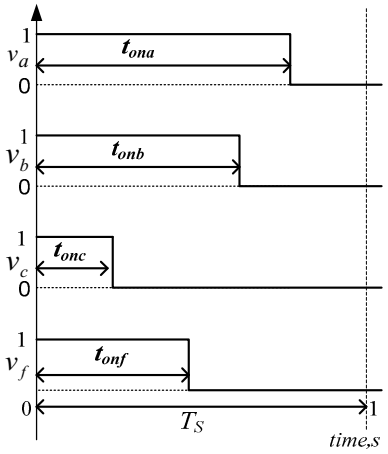

Figure 4. Output pulse width of one leg

In the 3D direct PWM, the integer part of v_{refj} determines the switching states of the corresponding leg in one PWM period; the fractional part of v_{refj} determines the pulse width. If the normalized reference voltage of the fourth-leg of a three-level VSI is 1.6, the switching states of the fourth-leg vary between S_f=1 and S_f=2 in one period, and the dwell time of S_f=2 equals 0.6*T_s. Therefore, the 3D direct PWM is likewise able to control multi-level four-leg VSIs.

III. GENERALIZED 3D DIRECT PWM

The 3D direct PWM for three-leg centre-split VSIs and four-leg VSIs from two-level to multi-level topologies is proposed. The detailed procedures for implementing the 3D direct PWM are provided in this section and the flow chart of the generalized 3D direct PWM is shown in Fig. 5. The shifting voltage must be used to determine the reference of each leg when four-leg inverters are controlled. A mode signal for indicating the inverter topology is needed, as illustrated in Fig. 5.The detailed procedures for implementing the generalized 3D direct PWM are as followings.

1) The input reference voltages are first shifted to the negative side of the dc bus and then normalized by voltage of one level. Normalization facilitates the following steps in the proposed 3D direct PWM.

$$\vec{v}_{ref} = \vec{V}_{ref}/E + V_n/E = \begin{bmatrix} V_{af}/E \\ V_{bf}/E \\ V_{cf}/E \end{bmatrix} + \frac{N-1}{2} \tag{19}$$

2) The reference voltage of each leg is then calculated.

$$v^*_{refj} = v_{refj} + v_{shift} \qquad j=a,b,c,f \tag{20}$$

where N is the number of the level of the VSI, and the shifting voltage is defined as:

$$v_{shift} = \begin{cases} 0 & \text{mode}=0 \quad 3\text{—leg centre—split VSI} \\ -(v_{\max}+v_{\min})/2 & \text{mode}=1 \quad \text{Four—Leg VSI} \end{cases} \tag{21}$$

where $v_{\max}$ is the maximum number from among v_{af}, v_{bf}, v_{cf} and v_{ff}; $v_{\min}$ is the minimum number from among v_{af}, v_{bf}, v_{cf} and v_{ff}, in which v_{ff} always equals zero.

3) The obtained reference voltage of each leg is decomposed. For an N-level inverter, its output switching state of each leg varies among 0 to N-1. The integer part determines the output switching states S_j and S_j +1; the fractional part determines the pulse width, i.e. the dwell time of S_j +1.

$$S_j = v_{offsetj} = Int(v^*_{refj}) \qquad j=a,b,c,f \tag{22}$$

$$t_{onj} = v^*_{refj} - v_{offsetj} \qquad j=a,b,c,f \tag{23}$$

4) According to the switching states and dwell times, the switching patterns are determined. The final trigger signals of each switch of one inverter leg are then generated.

By applying the trigger signals to the power switches, the VSIs generate the output voltages according to the given references. Hence, the three-phase four-wire voltage source inverters could be controlled by the proposed generalized 3D direct PWM.

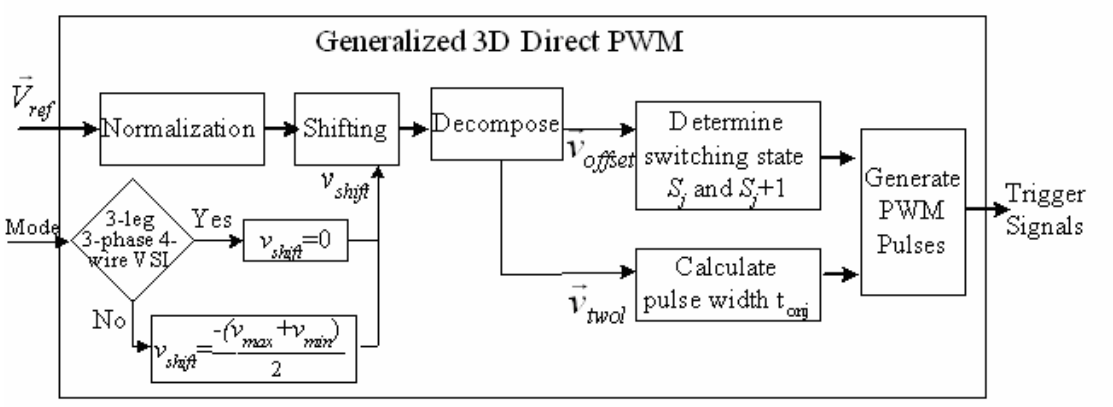

Figure 5. Flow chart of the generalized 3D direct PWM

IV. APPLICATION OF 3D DIRECT PWM IN THREE-PHASE FOUR-WIRE APFS

The proposed 3D direct PWM is first used to control a two-level four-leg VSI in a three-phase four-wire active power filter. The system configuration is shown in Fig.6. The three-phase balanced non-linear loads are shown in Fig.7, which are used to test the performance of the active power filter.

The output compensating currents references of the APF are calculated by instantaneous reactive power theory [12]. Since the proposed 3D direct PWM control the VSI to trace a voltage references, the reference currents are transformed to the reference voltage vector of the VSI. The reference voltage vector at time *KT* is calculated by (24) [17], where *K* indicates an arbitrary time instant. The *T* in (24) is the fixed sampling period of the control system and *T* equals 5kHz in simulation.

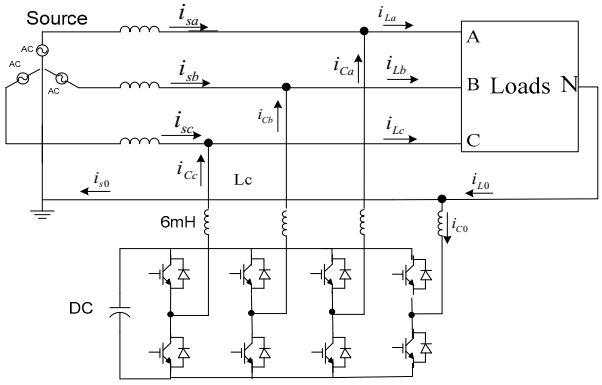

Figure 6. System configuration of APF using a two-level four-leg VSI

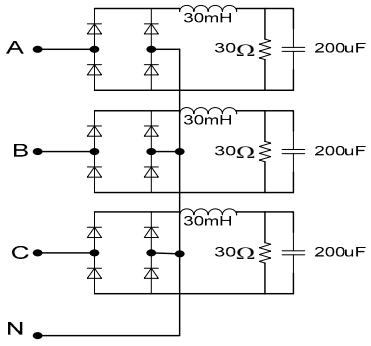

Figure 7. Three-phase balanced non-linear loads

$$\vec{v}[KT] = \vec{v}_S[KT] - \frac{R_c}{\Delta X}\left\{\vec{i}_c^{\,*}[KT] - (1-\Delta X)\vec{i}_c[KT]\right\} \quad (24)$$

where $\Delta X = \frac{R_c}{L_c} \cdot e^{-\frac{R_c}{L_c}T} \cdot T$.

The simulation models are built by using PSCAD/EMTDC. The phase-to-neutral voltage of the main system is 110V and three-phase balanced non-linear loads are supplied. The dc bus voltage of the active filter is 300V. The proposed 3D direct PWM is applied to control a two-level four-leg inverter in order to compensate the current harmonics, reactive power and neutral currents simultaneously.

The load currents and source currents after compensation are shown in Figs. 8 and 9 respectively. The total harmonics distortion (THD), power factor at the source and load sides and root mean square (RMS) values of the neutral currents are listed in Table I. According to the given simulation results, the validity of the APF in Fig.6 for compensating current quality is proved.

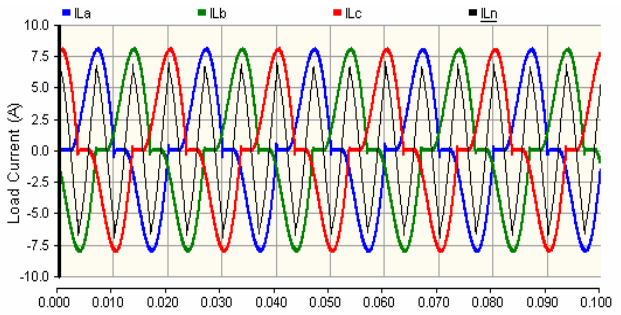

Figure 8. Load currents

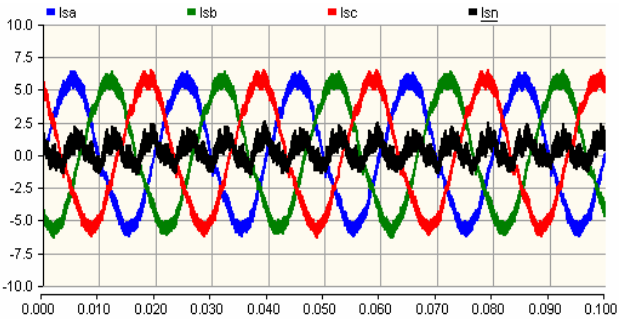

Figure 9. Source currents after compensation by APF

TABLE I. COMPENSATION PERFORMANCE OF APF

		A	B	C	Neutral
THD	Load currents	31.3%	31.0%	31.0%	3.98A
	Source currents after compensation	6.69%	7.14%	6.58 %	0.82A
Power Factor	Load currents	0.82	0.82	0.82	
	Source currents after compensation	0.999	0.999	0.999	

V. APPLICATION OF 3D DIRECT PWM IN THREE-PHASE FOUR-WIRE HYBRID FILTERS

The 3D direct PWM is also used to control a two-level three-leg centre-split inverter in a hybrid filter in three-phase four-wire systems. The system configuration of the hybrid filter is shown in Fig. 10, and the non-linear loads in Fig.7 are also used for testing the hybrid filter.

The simulation models of the hybrid filter are also built by using PSCAD. The parameters of the inductor and capacitor are selected to oscillate at 250Hz, i.e., 5th harmonics compared to 50Hz fundamental frequency component. The LC passive filter and the voltage source inverter are connected in series, so that the dc bus voltage of the VSI could be greatly reduced in a hybrid filter.

The parameters of the main system are the same as those for testing the pure active filter. However, the dc bus voltage of the VSI of the hybrid filter is only 50V, which is much lower than that for a pure active power filter. The reference voltage of the VSI needs to be calculated in order to apply the 3D direct PWM. The reference voltage for controlling the three-leg centre-split inverter in the hybrid filter is calculated by (25) according to the algorithm proposed in [18].

$$v_{jf} = k \cdot i_{shj} \quad j=a,b,c, \tag{25}$$

where i_{shj} is the harmonic components of the source currents, which could be determined by instantaneous reactive power theory. The value of k is 24 in simulations.

The 3D direct PWM is applied to control the output voltage of the centre-split VSI to follow the references. The control frequency is also 5kHz. The source currents after compensation are shown in Fig.11. The corresponding parameters of load currents and source currents after compensation are listed in Table II. Results indicate that current harmonics, reactive current and neutral currents are compensated simultaneously by the hybrid filter. In addition, the performance of the hybrid filter and the pure active filter are almost the same.

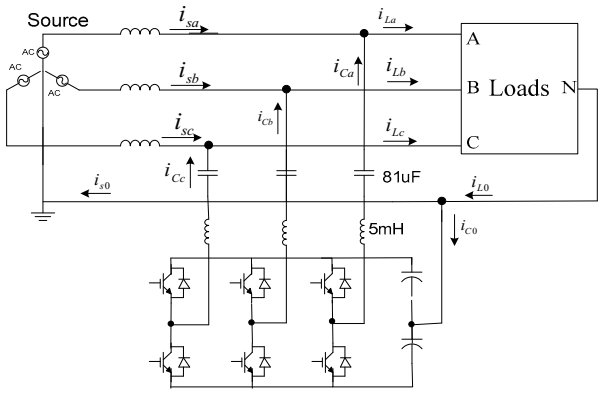

Figure 10. System configuration of the hybrid filter

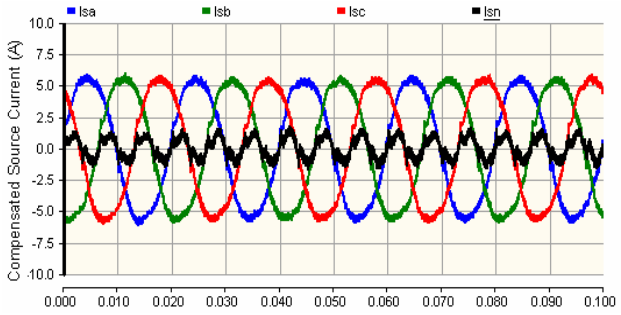

Figure 11. Source currents after compensation by hybrid filter

TABLE II. COMPENSATION PERFORMANCE OF THE HYBRID FILTER

		A	B	C	Neutral
THD	Load currents	31.3%	31.0%	31.0%	3.98A
	Source currents after compensation	6.86%	7.14%	7.09%	0.80A
Power Factor	Load currents	0.82	0.82	0.82	
	Source currents after compensation	0.994	0.995	0.994	

In the simulation model of the hybrid filter, the dc bus voltage of the voltage source inverter is only 50V. Hence, the rating of the active part in a hybrid filter is much lower than that for a pure active filter and the initial cost of the hybrid filter is lower. Moreover, the switching losses and EMS problem can be lessened. However, the hybrid filter requires more passive components and increases the volume of the whole filter.

VI. CONCLUSIONS

The 3D direct PWM for three-leg centre-split VSIs and four-leg VSIs is proposed in this paper. The proposed 3D direct PWM is also based on the voltage second approximation as the conventional SVM. However, it greatly reduces the computational cost. The detailed procedures for implementing a generalized 3D direct PWM for three-phase four-wire VSIs from two-level to multi-level topologies are given. In order to show its validities, the proposed 3D direct PWM is applied to control a four-leg inverter in an APF and a three-leg centre-split inverter in a hybrid filter in three-phase four-wire systems. Simulation models are implemented by PSCAD/EMTDC. Results indicate that the current harmonics, reactive power and neutral current could be compensated simultaneously when the proposed 3D direct PWM is used to control the three-phase four-wire VSIs to trace the references.

ACKNOWLEDGMENT

The authors would like to thank *the Science and Technology Development Fund, Macao SAR Government* and *University of Macau* for their financial supports.

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