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Quasi-Resonant DC Link Control of 3-Dimensional Hysteresis Current PWM Technique in 3-Phase 4-Wired Power Quality Compensator

Ming-hui Zhan Man-chung Wong Ying-duo Han

Abstract-- **In this paper, Quasi-Resonant DC Link (QRDCL) soft-switching 3-dimensional hysteresis current control for power quality compensator is investigated. Power quality compensator here is the shunt active power filter in the 3-phase 4-wire system to compensate the imbalance, reactive power, harmonics and neutral current. The 3-dimensional hysteresis current PWM technique changes the system frame from $a-b-c$ coordinate to α-β-0 coordinate for the purpose of controlling the neutral current individually in the 3-phase 4-wire system. And the quasi-resonant DC link soft-switching technique improves the performance of system with higher switching frequency and lower switching losses, etc. and enhances the PWM capability with inherent variable position and time interval of zero-voltage. The easy time sequence matching simplifies the system control and the results of simulation verified by the software PSCAD/EMTDC are found to be satisfactory to eliminate the switching losses without affecting the performance of power quality compensator.**

Index Terms-- **Hysteresis Current Control, Power Quality, Soft-Switching, 3DPWM**

I. Introduction

SOFT-SWITCHING inverter techniques have gained increasing interest over the last two decades due to the reduction or virtual elimination of switching losses that can be achieved. This also leads to the possibility of higher switching frequency, reduced heat-sink size and needless of snubber circuit due to the moderate dv/dt and di/dt, further to improve the system electro magnetic interference (EMI) performance. However, the initial several resonant soft-switching circuits force the change of inverter switch status only take place at fixed instants which makes the application of pulse width modulation (PWM) impossible [1]~[2], and the delta modulation for these circuits induces undesirable sub-harmonics in the voltage output spectrum that may give rise to rather high low-frequency current components. Hence, it would be desirable to combine soft-switching techniques with the superior harmonic performance of PWM at switching frequency much higher than obtainable in the past. The quasi-resonant DC link (QRDCL) circuit in this paper, as one of the resonant DC link circuits, has the inherent capability of variable selection of zero-voltage position and interval time, on which the conventional PWM techniques could apply and no sub-harmonic problems exist.

Among the various PWM control techniques, the hysteresis current control is popularly adopted because of its simplicity of implementation. Besides, fast-response current loop and inherent peak current limiting capability and the technique doesn't need any information about system parameters [3]. Due to the circuit configuration changed from 3-leg inverter in the 3-phase 3-wire system to the 3-leg center-spilt inverter in the 3-phase 4-wire system with the neutral line connected to the mid-point of the DC link capacitors, the conventional $a-b-c$ hysteresis current control is developed into α-β-0 hysteresis current control under the coordinate transformation from $a-b-c$ to α-β-0 for the purpose of controlling the neutral current individually in the 3-phase 4-wire system.

The easy time sequence matching is also developed to simplify the system control through detecting the rising edge of command switching signal of inverter and then coordinate the inverter and quasi-resonant DC link circuit. Fig. 1 shows the structure of 2-level 3-leg DC link center-split soft-switching inverter as power quality compensator in 3-phase 4-wire system to compensate the current issues such as the unbalance, reactive, harmonics and neutral currents.

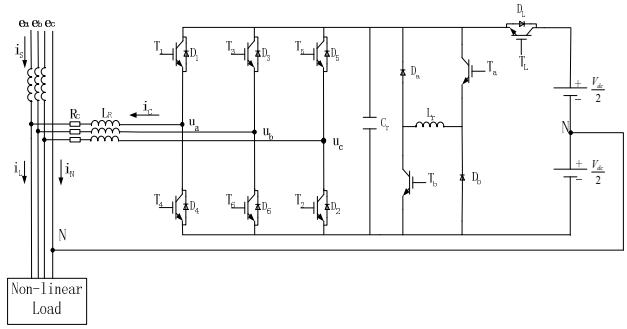

Fig. 1 2-level quasi-resonant 3-leg split DC link inverter as a power quality compensator

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The focus of the proposed QRDCL 3-dimensional hysteresis current PWM control is to investigate the influences of the soft-switching technique to 3-dimensional hysteresis current PWM control of power quality compensator in the 3-phase 4-wire system. Under the proposed control, the switching losses are eliminated obviously and the power quality compensator may operate at higher switching frequency and the system performance is improved, too. The simulation results verified by the PSCAD/EMTDC are also presented.

II. Basic Principles

A. 3-Dimensional Hysteresis Current PWM Control [4]

The neutral current, a serious problem to be handled, is not zero in the 3-phase 4-wire system under the unbalanced load. In order to control the neutral current individually, we can make the coordinate transformation to achieve this aim. The instantaneous current in α-β-0 can be transformed from a-b-c frame by matrix [P], such as shown in (1)

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} = [P] \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \qquad (1)$$

where

$$[P] = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix}$$

When the instantaneous equivalent current vector $\vec{i}$ is considered in α-β-0 frame, it can be expressed as (2).

$$\vec{i} = i_\alpha \vec{n}_\alpha + i_\beta \vec{n}_\beta + i_0 \vec{n}_0 \qquad (2)$$

The $\{\vec{n}_\alpha, \vec{n}_\beta, \vec{n}_0\}$ forms a basis and they are orthogonal to each other such that $\vec{n}_\alpha \bullet \vec{n}_\beta = \vec{n}_\beta \bullet \vec{n}_0 = \vec{n}_0 \bullet \vec{n}_\alpha = 0$. The basic concept of this control strategy is explained in Fig. 2.

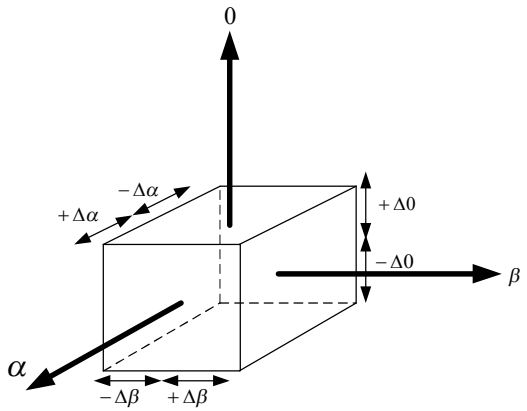


Fig.2 Concept of α-β-0 hysteresis control strategy

In 3-dimensional hysteresis current PWM control, there are 3 different hysteresis limits in 3 different α, β and 0 frames. If the hysteresis limits for Δα, Δβ and Δ0 are equaled to each other (Δα = Δβ = Δ0), the cubical hysteresis control technique can be achieved. There are 3 levels {1, 0, -1} in this cubical hysteresis control method and the sign of triggering pulses is an important parameter in tracking the current reference so as to choose the correct vectors. When the difference between the reference signal and actual input signal is larger than the hysteresis limited value, it will trigger to positive or, vice versa, to negative one according to its direction. However, when the difference is less than the hysteresis limit, there will be zero level.

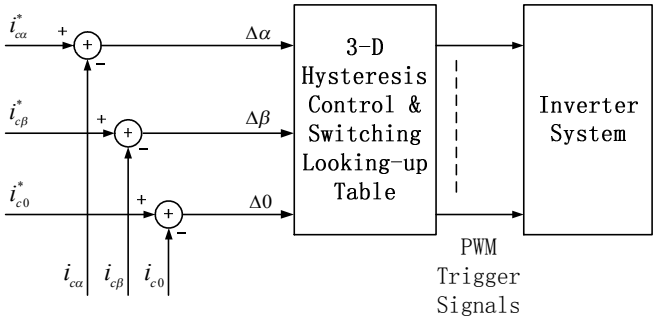


Fig. 3 Control block diagram

The control block diagram is illustrated in the Fig. 3, in which the injected current of the inverter is detected and transferred from a-b-c frame into α-β-0 frame. The difference between the command current $\left(i^*_{\alpha\beta0}\right)$ and the real compensating current $\left(i_{c\alpha\beta0}\right)$ will be the control signal $\left(\Delta i_{\alpha\beta0}\right)$ to the controller to control the action of inverter.

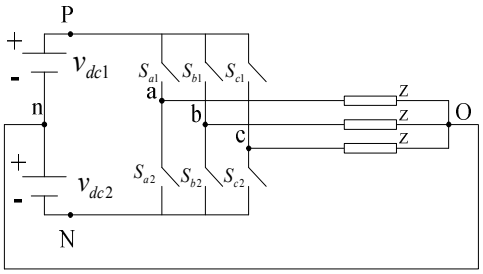


Fig. 4 Two-level three-leg center-split converters

Referring to the Fig. 4, it's assumed that the DC-linked upper-arm and lower-arm voltage of the inverter are equal to each other, i.e., $V_{dc1} = V_{dc2} = V_{dc}$. Due to the concept of the switching function as (3) and a-b-c frame transformation as (4), the instantaneous equivalent voltage vector can be given as (5).

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = v_{dc} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} \qquad (3)$$

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} = v_{dc}\sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} = v_{dc}\sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} \qquad (4)$$

$$\vec{v} = V_{dc}\left[\sqrt{\frac{2}{3}}\left(S_a - \frac{1}{2}S_b - \frac{1}{2}S_c\right)\cdot\vec{n}_\alpha + \frac{1}{\sqrt{2}}(S_b - S_c)\cdot\vec{n}_\beta + \frac{1}{\sqrt{3}}(S_a + S_b + S_c)\cdot\vec{n}_0\right] \qquad (5)$$

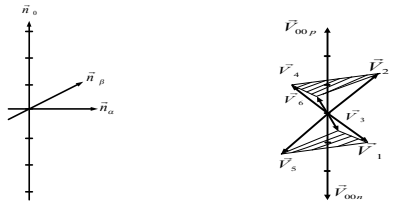
Where $S_x \in \{1,-1\}$ in 2-level system and x can be a, b and c.

Refer to (5), the values of switching vectors S_α, S_β and S_0 can be expressed as (6), (7) and (8) respectively.

$$S_\alpha = S_a - \frac{1}{2}S_b - \frac{1}{2}S_c \qquad (6)$$

$$S_\beta = S_b - S_c \qquad (7)$$

$$S_0 = S_a + S_b + S_c \qquad (8)$$



(a) (b)

Fig. 5 Basis $\{\vec{n}_\alpha, \vec{n}_\beta, \vec{n}_0\}$ (a) and 3DPWM voltage vectors (b)

	S_a	S_b	S_c	S_α	S_β	S_0
$\vec{V}_1$	1	-1	-1	2	0	-1
$\vec{V}_2$	1	1	-1	1	2	1
$\vec{V}_3$	-1	1	-1	-1	2	-1
$\vec{V}_4$	-1	1	1	-2	0	1
$\vec{V}_5$	-1	-1	1	-1	-2	-1
$\vec{V}_6$	1	-1	1	1	-2	1
$\vec{V}_{00p}$	1	1	1	0	0	3
$\vec{V}_{00n}$	-1	-1	-1	0	0	-3

TABLE 1
2-level 3DPWM voltage vectors in α-β-0 coordinate

There are totally 8 voltage vectors in 2-level inverter. With (4), (5) and (6), the switching vectors in α-β-0 frame are shown in Table 1. As illustrated in Fig. 5 (a), in α-β-0 coordinate, the $\{\vec{n}_\alpha, \vec{n}_\beta, \vec{n}_0\}$ forms the basis and the voltage vectors' allocation in 3-dimensional aspect are also shown in Fig. 5 (b) in terms of (5) and Table 1.

As there are 3 voltage levels {+, -, 0} for each voltage vector in the α-β-0 frame, the total voltage vectors is 2^3 or 27, however, there are only 8 voltage vectors we can use. Therefore, some conditions should be considered for choosing the proper voltage vector in the α-β-0 frame. The switching table for 2-level system just as Table 2 shows could be determined under the following conditions:

1) If the selected voltage vector has error in one axis, select the voltage vector having compensated error in the zero sequence.

2) If $S_\alpha = S_\beta = S_0 = 0$, as there are no all zero vectors in 2-level system, the vector selection is determined by Δi_0. If $\Delta i_0 \geq 0$, $\vec{V}_{0p}$ can be selected. If $\Delta i_0 < 0$, $\vec{V}_{0n}$ will be selected.

	$S_\alpha S_\beta S_0$	$S_a S_b S_c$		$S_\alpha S_\beta S_0$	$S_a S_b S_c$
1	+ + +	1 1 -1	15	- - 0	-1 -1 1
2	+ + -	1 1 -1	16	- 0 +	-1 1 1
3	+ + 0	1 1 -1	17	- 0 -	-1 1 1
4	+ - +	1 -1 1	18	- 0 0	-1 1 1
5	+ - -	1 -1 1	19	0 + +	1 1 -1
6	+ - 0	1 -1 1	20	0 + -	-1 1 -1
7	+ 0 +	1 -1 -1	21	0 + 0	1 1 -1
8	+ 0 -	1 -1 -1	22	0 - +	1 -1 1
9	+ 0 0	1 -1 -1	23	0 - -	-1 -1 1
10	- + +	-1 1 -1	24	0 – 0	1 -1 1
11	- + -	-1 1 -1	25	0 0 +	1 1 1
12	- + 0	-1 1 -1	26	0 0 -	-1 -1 -1
13	- - +	-1 -1 1	27	0 0 0 $\Delta i_0 \geq 0$	1 1 1
14	- - -	-1 -1 1	28	0 0 0 $\Delta i_0 < 0$	-1 -1 -1

Table 2 Switching table of 2-level system

B. Quasi-Resonant DC Link Commutation

To solve the shortcomings of voltage source type hard switching inverter such as low switching frequency, high switching losses, high EMI and acoustic noise, etc. Many types of resonant DC-link inverter using various soft-switching techniques have been studied [5]~[8]. The parallel resonant DC link inverter as one of the quasi-resonant DC link inverters has the minimum voltage stresses and allow variable zero voltage position and variable zero voltage duration which greatly enhances the PWM capability.

The circuit configuration of the quasi-resonant DC link (QRDCL) inverter is illustrated as Fig. 6, on the assumption that the resonant inductor L_r is much smaller than the load inductor, hence, the load current can be treated as a constant current source I_o during a switching period. The QRDCL consists of three switching devices T_a, T_b and T_L, two diodes D_a and D_b, resonant inductor L_r and resonant capacitor C_r. Fig. 7 shows the operation waveforms of the resonant components. As Fig. 6 & 7 illustrated, the zero-voltage time and position is controllable through controlling the conducting time of auxiliary switches T_a and T_b and the instant selection of t_0 which greatly enhances the PWM control capability.

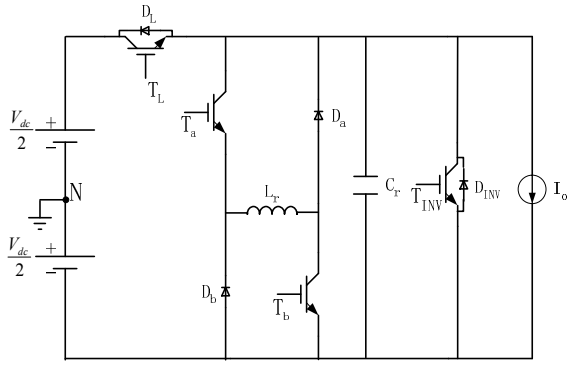


Fig. 6 The circuit configuration of the quasi-resonant DC link inverter

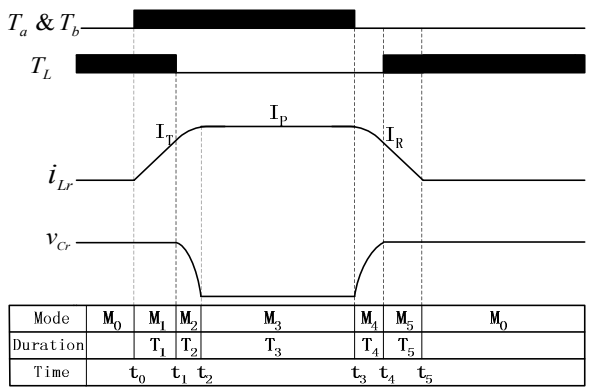


Fig. 7 The operation waveforms of the resonant process

The quasi-resonant DC link commutation operation could be divided into six operational modes and is generally depicted as follows:

Mode 0: (T_L: ON, T_a & T_b: OFF)

This mode is normal operation mode in which the load current I_o is flowing through T_L.

Mode 1: (T_L: ON, T_a & T_b: ON)

To operate DC link robustly, it requires initial inductor current. The T_a and T_b are turned on with zero current switching, then the resonant inductor current i_{Lr} increases linearly to the desired value I_T.

Mode 2: (T_L: OFF, T_a & T_b: ON)

When the switch T_L is turned off with zero voltage condition, the L_r and C_r circuit resonates with initial current I_T.

Mode 3: (T_L: OFF, T_a & T_b: ON)

The very moment the resonant capacitor voltage v_{Cr} reaches zero, the resonant inductor current is freewheeling through the paths $T_a - D_a$ and $T_b - D_b$.

Mode 4: (T_L: OFF, T_a & T_b: OFF)

To return the capacitor voltage v_{Cr} to the source voltage V_{dc}, the switches T_a and T_b are turned off with zero voltage condition.

Mode 5: (T_L: ON, T_a & T_b: OFF)

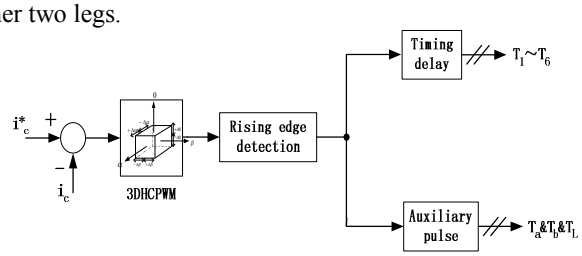
When the resonant capacitor voltage v_{Cr} is larger than the source voltage V_{dc}, the capacitor voltage is clamped to the source voltage V_{dc} and switch T_L is turned on under zero voltage condition. The remained energy in the resonant inductor is returned to the voltage source through the back-parallel diode of T_L.

C. Soft-Switching Control

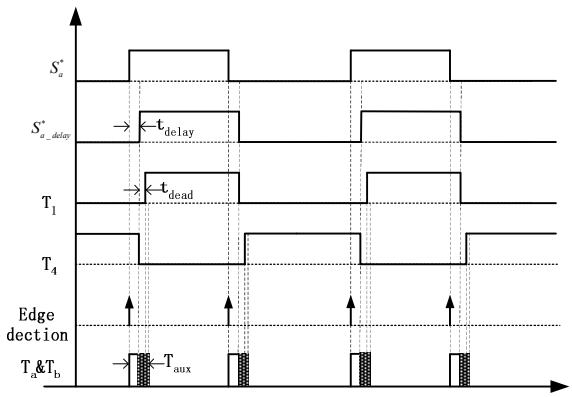
The matching of the main inverter circuit and resonant soft-switching circuit is the key point discussed here. As Fig. 7 shows, there is an interval (T_1 + T_2) before the resonant capacitor voltage v_{Cr} reaches zero. To simplify the control, the delay of time sequence of the main circuit is considered, which makes the switches turn-on and turn-off under the zero voltage condition. Fig. 8 shows the control block diagram of the proposed control and its gate signals for soft-switching operations. The dead time (t_{dead}) between upper and lower leg is also considered for analytical convenience and can be eliminated in reality. The switching control signals are obtained from the 3-dimensional hysteresis current PWM control, along with the rising edge detection block, which is then divided into two parts: one for timing delay (t_{delay}) of main circuit signals for the purpose of matching sequence of the soft-switching control; another is to trigger the control of the soft-switching circuit. To ensure the switching incidents be under the zero-voltage condition, the timing delay for the main circuit signal should be no less than the startup time needed for zero-voltage of the soft-switching circuit, which could be also indicated as:

$$t_{delay} \geq T_1 + T_2$$

If the conducting time of T_a and T_b is larger than the sum of timing delay t_{delay}, the turn-off time of lower-leg switch T_4 and turn-on time of upper-leg switch T_1, the switches of one leg can be turn-on and off under the zero-voltage, the same for the other two legs.



(a)



(b)

Fig. 8 Block diagram of soft-switching control. (a) soft-switching control scheme. (b) gate signals

III. SIMULATION VALIDATION

Table 3 shows the system simulation parameters of the circuit constructed as Fig. 1 with the simulation software (PSCAD/EMTDC). The source is selected to be 3-phase balance voltage source and the load is three single phase rectifier which will drive unbalanced and nonlinear currents.

Table 3 System simulation parameters

Parameter	Symbol	Value
AC voltage (phase, rms)	Vs	110 V
AC voltage frequency	fo	50 Hz
Filter inductance	L	12.5 mH
DC command voltage	Vdc	400 V
Switching frequency	fs	20 kHz
Hysteresis bandwidth	$\Delta B_{\alpha\beta 0}$	0.5 A
Resonant inductance	Lr	20 uH
Resonant capacitor	Cr	0.05 uF

As is shown in Fig. 9, the load current is not sinusoidal owing to the non-linear load and the source current is compensated to the sinusoidal one, in phase with the source voltage after the application of the power quality compensator.

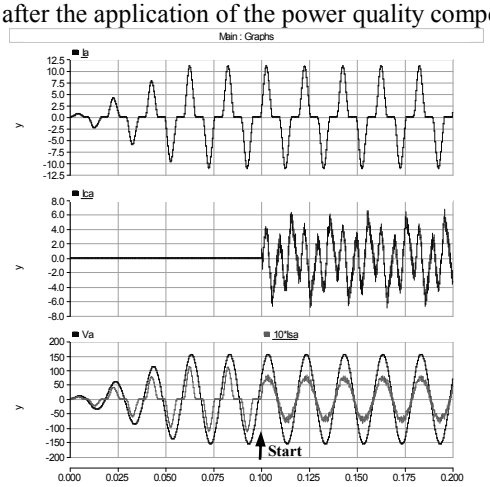
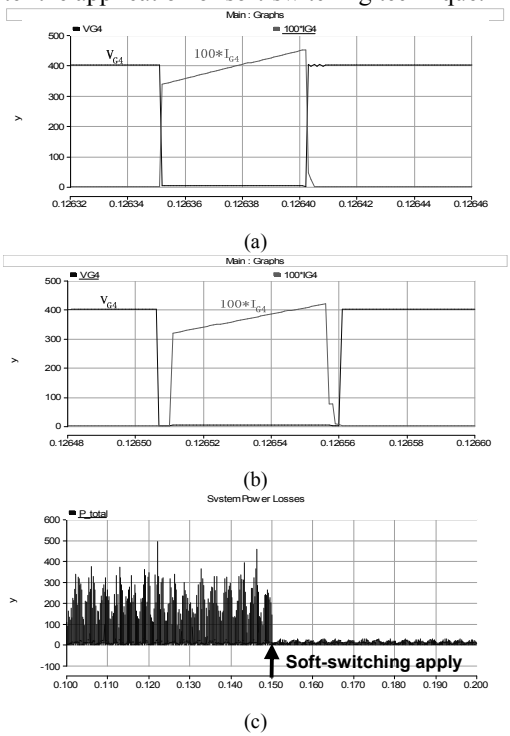


Fig. 9 Single phase voltage and current in active power filter mode

Fig. 10 shows the waveforms of the voltage, current and total power losses of system with and without QRDCL control. As illustrated in the Fig. 10 (a), the voltage and the current overlaps before the application of soft-switching technique, hence, instantaneous massive power dissipation happens. After the application of the soft-switching technique, the voltage and current staggers as shown in Fig. 10 (b), therefore, the instantaneous switching losses are eliminated. Fig. 10 (c) shows the total power dissipation of the inverter, the instantaneous power dissipation always reaches several hundreds before the application of soft-switching technique and reduced to several dozens as only on-state power losses exist after the application of soft-switching technique.



(a)

(b)

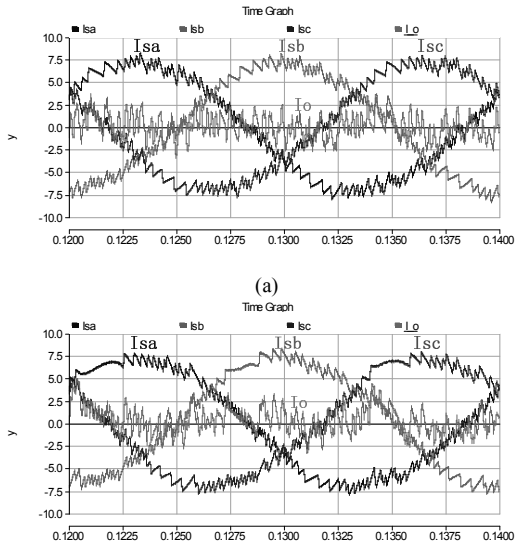
(c)

Fig. 10 Voltage and current waveforms with (a) and without (b) QRDCL and total power losses (c) with and without QRDCL

The waveforms of compensated source current, neutral current and the comparison of Total Harmonic Distortion (THD) before and after QRDCL application are are illustrated in Fig. 11 and Table 4, respectively. In order to investigate the neutral current, a new index named the average absolute error between the command value and the actual value of the neutral current in one period is proposed:

$$J_N = \frac{1}{T}\int_0^T \left|\Delta i_N\right| dt$$

From Fig. 11 and Table 4, the performance of the power quality becomes worse after the application of soft-switching technique, however, the variation is within the desirable range, besides with higher switching frequency, which validates the feasibility of the quasi-resonant DC link 3-D hysteresis current PWM control technique. Under the proposed control, the switching losses are decreased tremendously and the EMI & acoustic problems are further lowered.



(a)

(b)

Fig. 11 The compensated source & neutral currents with (a) and without (b) soft-switching technique

Table 4 Comparison of THD with and without QRDCL technique

	THD% & J	
Phase	Without QRDCL	With QRDCL
A	6.67%	6.75%
B	7.31%	7.13%
C	7.08%	7.61%
J_N	1.14	1.18

IV. CONCLUSION

The quasi-resonant DC link soft-switching 3-dimensional hysteresis current PWM control for the power quality compensator in the 3-phase 4-wire system is investigated. Integrated with the quasi-resonant DC link circuit, the performance of power quality is improved with higher switching frequency, lower switching losses and lower EMI

problems. The variable position and time interval of zero-voltage of the QRDCL circuit enhances the PWM capability greatly and no sub-harmonic problems exist. Simplified time sequence matching between the soft-switching control and inverter control are considered to have convenient control of the whole system. The simulation results prove that the proposed control method in the paper is feasible without influencing the performance of the power quality compensator.

V. REFERENCES

[1] D.M. Divan, "The resonant dc link inverter – a new concept in static power conversion", *IEEE Trans. Ind. Appl.,* 25, 317-325, 1989

[2] M.D. Bellar, T. Wu, A. Tchamdjou, J. Madhabi, M. Ehsani, A review of soft-switched dc-ac converters, *International Journal of Industry Applications, IEEE Transactions on,* 34(4), 1998, 847-860

[3] Joachim Holtz, "Pulsewidth Modulation --- A Survey", *IEEE Transactions on Industrial Electronics,* Vol. 39, No. 5, Dec. 1992, pp. 410-420.

[4] M. C. Wong, Z. Y. Zhao, Y. D. Han, L. B. Zhao, "Three Dimensional Pulse-Width Modulation Technique in Three-Level Power Inverters for Three-Phase Four-Wired System", *IEEE Trans. on Power Electronics,* vol. 16, no. 3, pp. 719-725, May 2001.

[5] Malesani, L.; Tomasin, P.; Toigo, V.; "space vector control and current harmonics in quasi-resonant soft-switching PWM conversion" *Industry Applications Society Annual Meeting, 1994., Conference Record of the 1994 IEEE,* vol.2, pp. 1122-1129, 2-6 Oct. 1994.

[6] Kurokawa, M.; Rukonuzzaman, M.; Konishi, Y.; Iwamoto, H.; Nakaoka, M.; "Space voltage vector modulated three-phase voltage source soft-switching active power filter" *Power Electronics and Drive Systems, 1999. PEDS '99. Proceedings of the IEEE 1999 International Conference on* , vol. 2, pp. 996-1002, 27-29 July 1999.

[7] He, J.; Mohan, N.; Wold, B., "Zero-voltage-switching PWM inverter for high-frequency DC-AC power conversion" *Industry Applications, IEEE Transactions on* , vol. 29, issue 5, pp. 959-968, Sept.-Oct. 1993.

[8] Cho, J.G.; Kim, H.S.; Cho, G.H., "Novel soft switching PWM converter using a new parallel resonant DC-link" *Power Electronics Specialists Conference, 1991. PESC '91 Record., 22nd Annual IEEE ,* pp. 241-247, 24-27 June 1991.

VI. BIOGRAPHIES

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