Design Considerations of Coupling Inductance for Active Power Filters

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Abstract— **A method for calculating the coupling inductance of active power filters (APFs) is proposed in this paper. The current ripple is defined and its relationship with the coupling inductance value is deduced based on error analyses. Hence, the lower boundary of the inductor value could be determined from the current ripple limit. A method to estimate the upper boundary of the inductor value is also proposed based on the capability to track compensating current reference. It is suggested to select the coupling inductor value close to the lower boundary for the APF. The upper boundary is used to check if any further improvement is needed for getting the balance between tracking speed and suppressing current ripple. The converter topology and modulation signal scheme are also considered in selecting the coupling inductor. Simulation and experimental results are provided to show the validity of the proposed method. Comparisons with previous methods are also given. The proposed method may also work for other inductor-coupled system, such as STATCOM.**

Keywords-active power filter, coupling circuits, voltage source converter

I. INTRODUCTION

Active power filters (APFs) are widely used parallel power quality compensators for compensating current harmonics, reactive current and neutral currents in three-phase four-wire systems [1]-[3]. The basic structure of the APF is shown in Fig.1. A coupling inductance is connected between the point of common coupling (PCC) and the voltage source converter (VSC)

To select a proper coupling inductance is important for the APF, since it directly affects the output filtering and harmonic tracking capability. The design of coupling inductance was based on the capability of compensating reactive current and harmonic current in [3]-[5]. The application of this method is limited since load characteristics are needed for calculating the inductance, which are usually time-varying and sometimes unavailable.

Since only parameters from the APF are needed for calculating the inductance, the capability of suppressing output current ripple was used more often [3] [6]-[9]. Different methods are provided to estimate the inductor value for satisfying the current ripple limit. However, there is no clearly definition for the current ripple. The relationship between the current ripple and inductor value is only roughly estimated without error analyses. Hence, the accuracy of the obtained results could not be guaranteed. In addition, the effects of the converter topology and modulation signals on current ripple are overlooked in the past studies.

When both compensation capability and current ripple limit are considered, a range of coupling inductance is obtained [10]. However, the obtained upper boundary is frequently smaller than the lower boundary by using the method in [10]. Simulation tests may provide a straightforward method to determine the coupling inductance in the given range, but try-and-test process is usually time-consuming, especially for the beginners in this field. Hence, the method for determining coupling inductor of the APF needs to be improved.

In this paper, design method of the coupling inductance of the APF is studied. In session II, the current ripple is defined as the maximum difference between the compensating current and its reference in a pulse width modulation (PWM) period. The method of calculating the minimum coupling inductance to satisfy the current ripple limit is deduced based on the error analyses. The converter level and modulation signal are also considered when the coupling inductance is selected. The capability to track compensating current is used to deduce an upper boundary of the inductor value. Finally, a method for determining the proper coupling inductor of the APF is proposed in this session. In session III, simulation results are provided to show the validity and comparisons with previous methods are provided. Experimental results are provided in session IV.

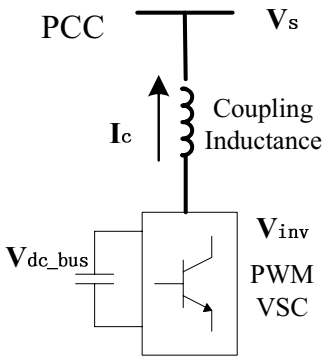

Figure 1. Basic structure of the APF

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II. METHOD FOR CALCULATING COUPLING INDUCTANCE

A. Suppress the current ripple

The coupling inductance of the APF could suppress the output current ripple. When the period of the PWM control is small enough, the current passing through the coupling inductor varies linearly, as given in (1) and illustrated in Fig.2.

$$\Delta I^* = \frac{v_{inv} - v_S}{L} \cdot T_S \quad , \tag{1}$$

where v_{inv} is the average output of the inverter in a switching period, v_S is the voltage at the PCC, and Ts is the period of PWM.

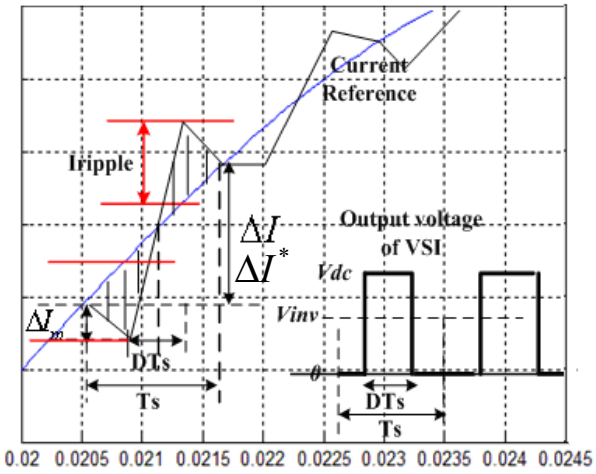

Figure 2. Current ripple and symmetrical-aligned modulation signal

When PWM is used to control voltage source converters, the output voltage of the VSCs always changes discontinuously. For example, the output voltage varies between *0* and V_{dc_bus} for a two-level VSI. As shown in Fig.2, the output voltage of the converter varies between two neighboring levels to synthesize the reference voltage. The average output voltage in each period equals to v_{inv}, as expressed in (2).

$$v_{inv} \cdot T_S = V_{dc} \cdot DT_S \tag{2}$$

Eq. (2) is for two-level VSI and it needs to be revised as (3) for a multi-level VSC [11]. It is assumed v_{inv} is in the range of V_{offset} to $V_{offset}+V_{dc}$. V_{dc} denotes voltage of each level, D is the duty ratio and V_{offset} is integer multiples of V_{dc}.

$$v_{inv} \cdot T_S = (V_{offset} + V_{dc}) \cdot DT_S + (1-D)T_S \cdot V_{offset} \tag{3}$$

For simplicity, (2) for two-level inverter is used hereinafter. However, it can be proved that all the deduced results also work for multi-level inverters. The source voltage is assumed to be a constant in a period. The current passing through the coupling inductor varies like a sawtooth wave. Symmetrical-aligned modulation signal is selected since it gives the lowest current ripple [12]. The current variation in a period is shown in Fig.2 and is expressed in (4).

$$\Delta I = \frac{-v_S}{L} \cdot \frac{1-D}{2} T_S + \frac{V_{dc} - v_S}{L} \cdot DT_S + \frac{-v_S}{L} \cdot \frac{1-D}{2} T_S \tag{4}$$

According to (2), the ΔI^* in (1) and ΔI in (4) are the same. Practically, dead-time during the switching, delay in the control system and errors in the inductor value generate errors between ΔI^* and ΔI. They may not match exactly as shown in Fig.2. All these factors are overlooked in this paper since they are not the main causes of the current ripple. The current ripple exists mainly due to the output voltage of the inverter changes discontinuously. As shown in Fig.2, the error between the compensating current and its reference are two shadowed area. Due to the symmetrical properties, the area of the two shadowed error area is the same and total error area is calculated by (5),

$$\begin{aligned} S_{error} &= 2[\frac{1}{2}\frac{T_S}{2}\frac{\Delta I}{2} + \frac{1}{2}(\frac{T_S}{2} + \frac{DT_S}{2})\Delta I_m - \frac{1}{2}\frac{DT_S}{2}(\frac{\Delta I}{2} + \Delta I_m)] \\ &= \frac{1}{2}T_S(\frac{1-D}{2}\Delta I + \Delta I_m) \end{aligned} \tag{5}$$

where ΔI_m is the change of the APF output current from 0 to *(1-D)Ts/2,* and $\Delta I_m = \frac{v_S}{L}\frac{1-D}{2}T_S$. Combined with (2) and (4), (5) could be further revised as:

$$S_{error} = \frac{T_S^2}{4L}(DV_{dc} - D^2 V_{dc}) \tag{6}$$

Since D is the duty ratio and varies from *0* to *1*, S_{error} increases as V_{dc} increases. According to (7), $\frac{dS_{error}}{dD}$ equals zero when D=1/2, i.e., the maximum value of S_{error} occurs when D=1/2.

$$\frac{dS_{error}}{dD} = \frac{T_S^2}{4L}(V_{dc} - 2DV_{dc}) = 0 \tag{7}$$

Current ripple is defined as (8), which is the maximum variation of the output current of the APF from the reference current in a period. According to (5), the relationship between the error area and current ripple is given in (9).

$$I_{ripple} = \Delta I_m + \frac{(1-D)}{2}\Delta I \tag{8}$$

$$S_{error} = \frac{1}{2}T_S I_{ripple} \tag{9}$$

When D=1/2 and the error area achieves the maximum value, I_{ripple} is

$$I_{ripple} = \frac{T_S V_{dc}}{8L}. \tag{10}$$

If the current ripple is set to be smaller than ΔI_r, (11) is obtained.

$$L \geq \frac{V_{dc}}{8 f_S \Delta I_r} \tag{11}$$

In addition, if left-aligned or right-aligned modulation is used instead of symmetrical-aligned modulation, the current ripple is shown in Fig.3. The error area is calculated by (12) and the corresponding current ripple is given in (13).

$$S_{error} = \frac{1}{2} T_S (\Delta I_r - D\Delta I) \tag{12}$$

$$I_{ripple} = \Delta I_r - D\Delta I \tag{13}$$

When D=1/2, I_{ripple} is

$$I_{ripple} = \frac{T_S V_{dc}}{4L} \tag{14}$$

The current ripple is doubled. Hence, the symmetrical-aligned modulation could reduce the current ripple without increasing the switching frequency. It is suggested to be adopted in APFs. For multi-level inverter $V_{dc} = V_{dc\_bus}/$ (*Level*-1), and (11) is revised as (15).

$$L \geq \frac{V_{dc\_bus}}{8(Level-1) f_S \Delta I_r} \tag{15}$$

Finally, (152) is employed for handling coupling inductor values in the following discussions.

B. Current tracking Speed

When only reactive current is compensated by the APF, the system voltage and output current of the APF are expressed as (16) and (17).

$$v_S = \sqrt{2} V_S \sin(\omega t) \tag{16}$$

$$i_{cfq} = \sqrt{2} I_{cfq} \sin(\omega t - 90^\circ) \tag{17}$$

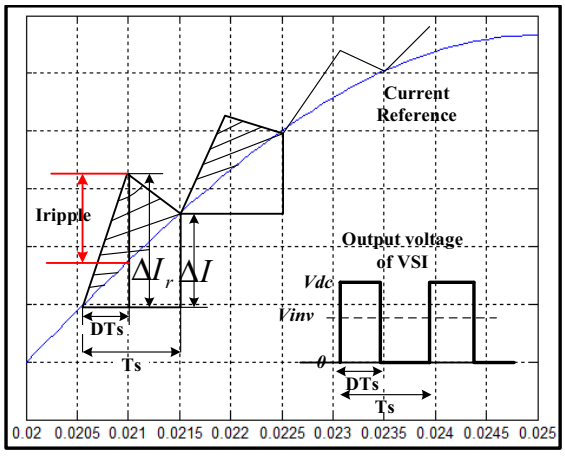

Figure 3. Current ripple and left-aligned modulation signal

The slope of the compensating current is (18).

$$\frac{di_{cfq}}{dt} = \sqrt{2} I_{cfq} \omega \cos(\omega t - 90^\circ) = \sqrt{2} I_{cfq} \omega \sin \omega t \tag{18}$$

The relationship between the coupling inductor and the slope of the compensating current is

$$\frac{di_{cfq}}{dt} = \frac{v_{inv} - v_S}{L} \,. \tag{19}$$

If the maximum value of the current slope in (18) could be achieved, the coupling inductor should satisfy (20).

$$L \leq \frac{v_{inv} - v_S}{\sqrt{2} I_{cfq} \omega} \tag{20}$$

According to (16) and (18), the source voltage reaches its peak when the slope of the compensating current reaches the maximum value. The voltages across the coupling inductor for tracking the maximum current slope of different types of VSC are listed in Table I. V_{dc_bus} is the dc voltage of the inverter and $V_{phase\_to\_neutral}$ is the root-mean-square (RMS) value of the phase-to-neutral voltage at PCC. A factor of two is divided for three-leg full bridge inverter and four-leg inverter, since two inductors exist in the phase-to-phase circuits. For simplicity, it is assumed $v_{inv} - v_S = \delta_v V_{dc\_bus}$ and (21) is obtained.

$$L \leq \frac{v_{inv} - v_S}{\sqrt{2} I_{cfq} \omega} = \frac{\delta_v V_{dc\_bus}}{\sqrt{2} \omega I_{cfq}} \tag{21}$$

δ_v could be estimated according to Table I, and the typical value of δ_v is in the range of 0.1~0.3.

When reactive current and current harmonics are compensated simultaneously by APF, the current slope is expressed as:

$$\frac{di_c}{dt} = \frac{di_{cfq}}{dt} + \frac{di_{ch}}{dt}, \tag{22}$$

where

$$\frac{di_{ch}}{dt} = \frac{d(\sum_{h=2}^{\infty} \sqrt{2} I_{ch} \sin(h\omega t - \varphi_h))}{dt} = \sum_{h=2}^{\infty} \sqrt{2} I_{ch} h\omega \cos(h\omega t - \varphi_h) \tag{23}$$

TABLE I. VOLTAGE DROP ACROSS THE INDUCTOR FOR DIFFERENT VSC

Converter topology	$v_{inv} - v_S$
Single-phase VSC	$V_{dc\_bus} - \sqrt{2} V_{phase\_to\_neutral}$
Three-phase full bridge VSC	$(V_{dc\_bus} - \sqrt{6} V_{phase\_to\_neutral})/2$
Three-leg center-split VSC	$V_{dc\_bus}/2 - \sqrt{2} V_{phase\_to\_neutral}$
Four-leg VSC	$(V_{dc\_bus} - \sqrt{6} V_{phase\_to\_neutral})/2$

Inequality in (24) needs to hold for tracking the maximum current slope.

$$L \le \frac{\delta_v V_{dc\_bus}}{\sqrt{2} I_{cfq} \omega + \sum_{h=2}^{\infty} \sqrt{2} I_{ch} h\omega \cos(h\omega t - \varphi_h)} \quad (24)$$

The maximum current slope varies with phase shift between the harmonic current and reactive current. It is also not feasible to include all the harmonics in (24). Practically, the simplified version (25) could be used to determine the upper boundary of the coupling inductance.

$$L \le \frac{\delta_v V_{dc\_bus}}{r I_c \omega} \quad (25)$$

I_c is the current rating of the APF and r is suggested to select the order of the most significant harmonics in the load currents. The value of r could be estimated without measuring the load currents. When the loads are mainly home or office appliances, which uses single-phase switch mode power supply, r should be three. If the load is a three-phase adjustable speed drive, r usually selects five.

C. Method for calculating coupling inductance

Combining the results of the previous two parts; the range of the coupling-inductance of an APF is expressed as (26). The detailed explanations for each parameter are given in Table II. The lower boundary is totally determined by the APF settings. The last two parameters in Table II vary with non-linear loads to be compensated and are used for estimating the upper boundary.

$$\frac{V_{dc\_bus}}{8 f_s (Level - 1) \Delta I_r} \le L \le \frac{\delta_v V_{dc\_bus}}{r \omega I_c}. \quad (26)$$

When the final value of the inductor is determined, it is suggested to select a value close to the lower boundary. The value close to the lower boundary could provide better current tracking speed with acceptable current ripples. A smaller inductor also reduces the cost. However, it is suggested to still test the final value by estimating the upper boundary according to (26). In some cases, the obtained upper limit of the inductor value is smaller than the lower limit. It indicates conflicts exist in the requirement of current tracking speed and suppressing current ripple. Some approaches, such as increasing PWM frequency and adopting multi-level VSI, could be considered to reduce the lower boundary. Another alternative solution is to use LC or LCL filter in the coupling circuits [13].

TABLE II. PARAMETERS FOR CALCULATING INDUCTOR VALUE

Parameter	Explanation	Example
Vdc_bus	DC bus voltage of the inverter	200V
Level	The level of the VSI	2 or 3
fs	PWM frequency	5000
Ic	Current rating of the APF (RMS)	5A
ω	Fundamental Frequency	314
ΔI_r	Maximum current ripple.	0.5A
δ_v	Typical value: 0.1 ~ 0.3	0.2
r	The order of the most significant harmonic	3

III. SIMULATION RESULTS

A. Compare coupling inductor values of APF using two-level VSC

Simulation models are built by using PSCAD/EMTDC. A two-level center-split voltage source converter is first used as the main circuit of the active power filter. The system configuration is shown in Fig.4. Parameters are listed in Table II and root mean square (RMS) value of source voltage V_s is 55V. Single-phase rectifiers are used as loads. Hence, the most significant harmonics are third order harmonic. In addition, symmetrical-aligned scheme is used in PWM method.

Formula for calculating the coupling inductor in [6][8][10] are given in (27)-(29) respectively.

$$\frac{3}{16} \cdot \frac{V_{dc\_bus}}{f_s \Delta I_r} \le L \quad (27)$$

$$\frac{V_{dc\_bus}}{6 f_s \Delta I_r} < L \quad (28)$$

$$\frac{\Delta V}{\omega I_{c\_\max}} \le L \le \frac{\Delta V}{4 \Delta I_r f_s} \quad (29)$$

where ΔV in (29) is the difference between the source voltage and the inverter voltage, which depends on the values of the DC link voltage and the modulation index, and $\Delta V = 0.2 V_{dc\_bus}$ is used in this paper.

The inductor values calculated by different methods are listed in Table III. The lower boundary is larger than upper boundary when both (26) and (29) are used. However, the error in the proposed method is much smaller. Since there is no discussion about how to select the inductor value inside the given range in [10]. The proposed method is much easier for the user to find a proper inductor value.

The total harmonic distortion (THD) of the load current is 30.8% and RMS of neutral current is 9.2A before compensation. THD of the source current and RMS value of neutral current after compensation are listed in Table III. Results indicate that the compensating performance is kept acceptable when the inductor is selected in the proposed range.

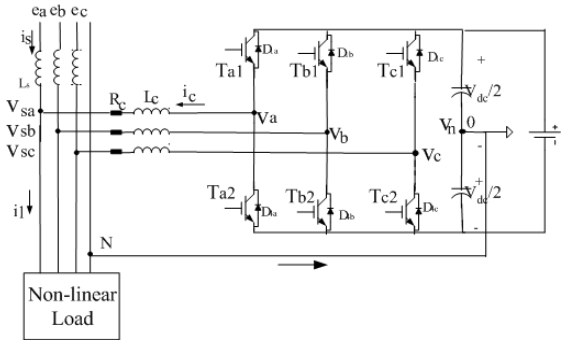

Figure 4. APF use two-level center-split converter

TABLE III. COUPLING INDUCTANCE AND COMPENSATION RESULTS FOR THE APF USING TWO-LEVEL INVERTER

Formula	L(mH)	THD	Neutral current
Eq. (17)	Lmin=15	9.7%	3.2A
Eq. (28)	Lmin=13.3	8.67%	2.8A
Eq. (29)	Lmin=18	10.7%	3.7A
	Lmax=5.7	6.39%	1.9A
Eq. (26)	Lmin=10	7.04%	2.2A
	Lmax=8.4	6.22%	1.9A

B. *Compare coupling inductor values of APF using three-level VSC*

In order to reduce the lower boundary of the inductor value, three-level center-split converter is used instead of the two-level inverter in the APF model. The system configuration is shown in Fig.5. The other settings are the same as those given in Table II. The lower boundary is reduced to 5mH by using the proposed method, as listed in Table IV. Since converter topology is not considered in [6][8] and [10], the inductor values are the same for these methods.

The simulation results of the APF using three-level VSC are given in Table IV. Results indicate that the proposed method could adjust the coupling inductor value according to the inverter topology, so that it is more general applicable than previous methods. Fig.6 shows the performance of the APF to track the compensating current reference for three different inductor values. A larger inductor value reduces the current tracking speed, while a smaller inductor value increases the current ripples. When inductor value is 5mH, the source currents are shown in Fig.7, in which the APF begins compensation at 0.04s.

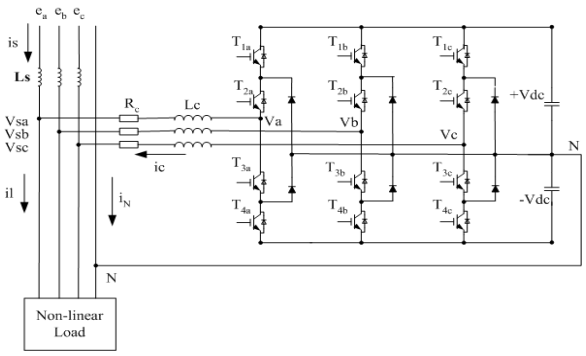

Figure 5. APF use three-level center-split converter

TABLE IV. COUPLING INDUCTANCE AND COMPENSATION RESULTS FOR THE APF USING THREE-LEVEL INVERTER

	L(mH)	THD	Neutral current
Eq. (17)	Lmin=15	9.4%	3.1A
Eq. (28)	Lmin=13.3	8.7%	2.8A
Eq. (29)	Lmin=18	10.6%	3.6A
	Lmax=5.7	6.0%	1.8A
Eq. (26)	Lmin=5	5.43%	1.6A
	Lmax=8.4	6.15%	1.9A

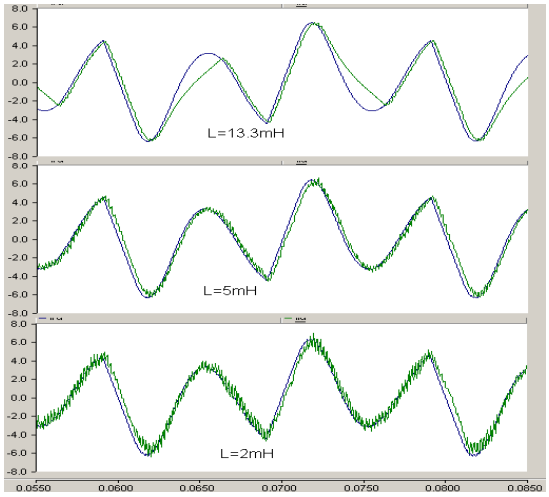

Figure 6. Output current and reference current of the APF using three-level inverter

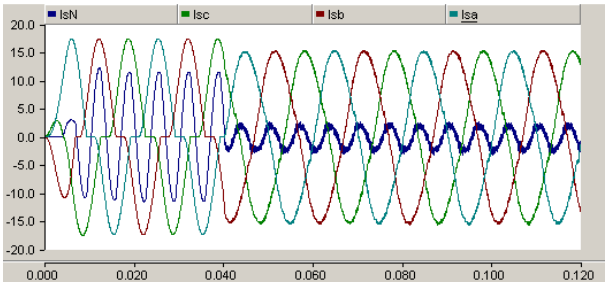

Figure 7. Source current when L=5mH

IV. EXPERIMENTAL RESULTS

A three-phase four-wire APF prototype is built, in which a three-level center-split VSC is used. The system configuration is shown in Fig.5. The parameters in Table I are used and coupling inductor is 5mH. The source current before compensation and after compensation together with the source voltage are shown in Fig.8. The corresponding parameters are listed in Table V.

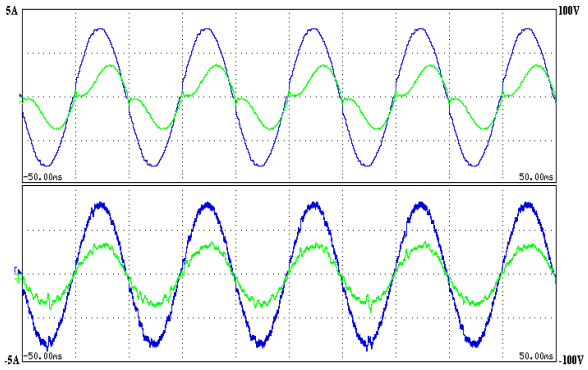

Figure 8. Experimental results

TABLE V. COMPENSATION PERFORMANCE

	THD	Power Factor	Displacement Power factor
Load Current	25.3%	0.84	0.89
Source Current	6.5%	0.98	1

V. CONCLUSIONS

A method for calculating the range of the coupling inductance of active power filters is proposed in this paper. The inductor value is suggested to select near the lower boundary, which is calculated according to the current ripple limit. The upper boundary is estimated according to compensation requirements, which could be used to decide if any further improvement is needed for reducing the current ripple. Simulation and experimental results are provided to show its validity. Comparisons with other methods are also provided. Results indicate that the proposed method has better accuracy and is more general applicable in selecting the coupling inductor of the APFs.

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