

Evaluation of Quasi-Resonant DC-Link Technique on Generalized Three-Level Inverter

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Abstract—This paper presents a combination of a quasi-resonant dc-link (QRDCL) inverter and a generalized three-level inverter. QRDCL inverter can decrease the dc-link voltage to zero in order to provide a zero voltage condition for the power devices. The voltage stresses of the power devices can be released and the switching losses of the inverter can be reduced under zero-voltage switching (ZVS). Generalized multilevel inverter topology provides an alternative way in high level inverter implementation. The generalized multilevel inverter is constructed by several basic cells which enable a higher flexibility in extending the levels of inverter, and moreover it gives the inverter a self voltage balancing ability without any assistance from extra circuits. Control strategy of a generalized three-level QRDCL inverter is proposed. Switching losses of the inverters are also presented to prove the feasibility of a generalized three-level QRDCL inverter.

I. INTRODUCTION

Three level inverters have been widely used in high-voltage medium-power application. The multilevel topology has attractive features which provide higher flexibility and stability for multilevel converters. Since the switching devices of a single-phase three-level inverter share half of the dc bus voltage, the voltage stresses across the switching devices are released in comparison with a two-level inverter. In addition, three-level inverters provide more available vectors that can improve the harmonic contents by selecting appropriate switching vectors [1]. Multilevel topology also allows the switching devices operate with a lower switching frequency since more steps are being generated in the output voltage. However, dc bus voltage unbalance has been one of the major problems of multilevel inverters. The unbalanced dc voltages of a three-level inverter could lead to a shifted voltage at the virtual ground. Different control strategies and circuit structures have been proposed in solving this problem [2]–[4]. Among them, the generalized multilevel inverter solved the problem by giving the inverter a self voltage balancing ability [5]. The generalized multilevel inverter is constructed by two or more basic cells which also provide a higher extensibility for the inverters.

In three-phase four-wire applications, the number of power devices of a three-level inverter is much more than that of a two-level inverter. The increase in number of power devices leads to the increase of switching losses. System instability, switching frequency limitation and electromagnetic interference are some of the problems which directly relate to the switching losses of the inverters. Therefore soft switching techniques have been proposed to tackle these problems in order to improve the efficiency and the performance of the inverter [6]. Resonant dc-link or quasi-resonant dc-link (QRDCL), resonant commutated pole, zero switching transition are the commonly used soft switching techniques [7]–[10], which have different characteristics in terms of number of auxiliary devices, control strategies and their soft-switched ability. QRDCL technique is employed in this paper since it has a simpler control system and lesser auxiliary components. Zero voltage condition is generated by QRDCL inverter while the dc bus voltage decreases to zero. Severe dv/dt of the power devices is relaxed and the overall switching losses are reduced under zero voltage switching (ZVS) of the devices. As dc voltage unbalance and serious switching losses could happen in a traditional multilevel inverter, a combination of QRDCL technique and generalized three-level inverter is proposed in this paper. Operating principles of both QRDCL and generalized three-level is given and the effects of their interaction are analyzed. Control strategy of a QRDCL generalized three-level inverter is also proposed and the switching losses of a tradition inverter and the proposed inverter are compared in the simulation.

II. SELF VOLTAGE BALANCING AND SOFT COMMUTATION

A. Generalized Multilevel Inverter

A generalized three-level inverter which is constructed by three basic cells is shown in Fig. 1. The basic cell is originally a traditional two-level inverter. By connecting the output of a two-level inverter to the dc bus of another two-level inverter, an inverter with any number of levels can be built. This cell structure of the generalized topology also equips the inverter with a self dc voltage balancing ability where modification on

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control system is not needed. The voltage unbalance is a major problem of multilevel inverter, this problem occurs when there is zero sequence current flowing through the dc bus. Therefore self voltage balancing is a compelling feature for multilevel inverter, especially for three-phase four-wire applications such as active power filter, which has higher possibility in facing zero sequence current. In addition, traditional diode-clamped and capacitor-clamped inverters can be derived from this generalized inverter topology. Table 1 shows the four possible switching combinations of a generalized three-level inverter and their corresponding connection of capacitors. When switches S1, S2 and S6 are turned on, positive dc voltage is produced. Capacitor Cm1 and Cm3 are connected in parallel and self balanced. As switches S3, S4 and S5 are triggered, capacitor Cm2 and Cm3 are connected in parallel and produced negative dc voltage. The connection of capacitor pair is changed alternately and results in voltage equality of capacitors Cm1, Cm2 and Cm3.

TABLE I. SWITCHING TABLE OF A GENERALIZED INVERTER

Output Voltage	S1	S2	S3	S4	S5	S6	Capacitors in Parallel
Vdc/2	1	1	0	0	0	1	Cm1 & Cm3
0	1	0	1	0	0	1	Cm1 & Cm3
0	0	1	0	1	1	0	Cm2 & Cm3
-Vdc/2	0	0	1	1	1	0	Cm2 & Cm3

B. Quasi-Resonant DC-Link Inverter

Fig. 2(a) shows the circuit structure of a quasi-resonant dc-link for three-level inverter. The QRDCL circuit is constructed by two symmetrical modules which can operate independently. The inductor Lr and the capacitor Cr are small energy storage devices. The voltage of capacitor Cr will decrease to zero when the energy in the capacitor transfers to the inductor. Once the zero voltage condition appears, the inverter's main switches are triggered and could achieve zero voltage turn on and turn off. Fig. 2(b) shows the resonant voltage and current of one of the QRDCL module correspond to the trigger signals of auxiliary switches Sa and Sc. The auxiliary switch Sa achieves zero current turn off when the resonant current crosses the zero point, and switch Sc is turned on under zero voltage condition when the resonant voltage returns to its original value. The resonant frequency of the QRDCL circuit can be controlled by adjusting the capacitance of Cr and the inductance of Lr, which can be obtained from

$$T = \pi \sqrt{L_r C_r} \quad (1)$$

The resonant current can also be calculated from

$$i_r = \frac{V_{dc}}{4} \sqrt{\frac{C_r}{L_r}} \sin\left(\frac{1}{\sqrt{L_r C_r}} t\right) \quad (2)$$

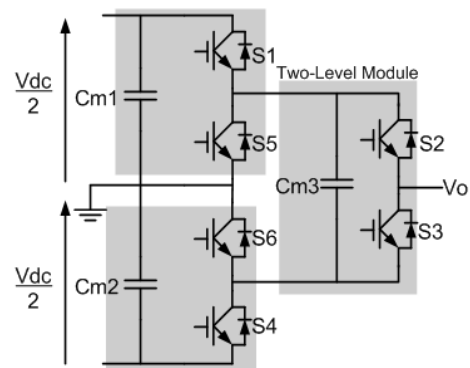
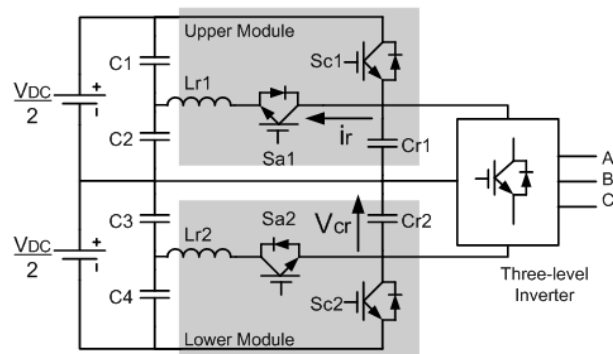
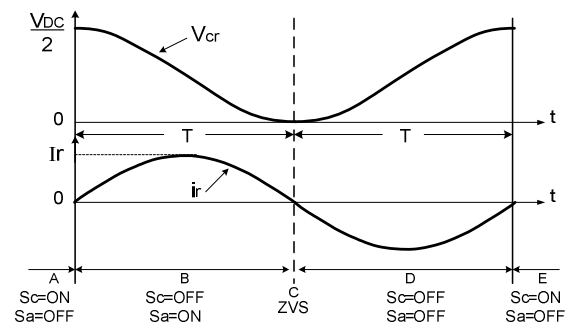


Figure 1. Generalized three-level inverter.



(a)



(b)

Figure 2. (a) Quasi-resonant dc-link modules, and (b) the corresponding resonant waveforms.

Detail analysis and operations of the QRDCL circuit can refer to [8]. The features of QRDCL can be summarized as follows.

- Both inverter's main switches and auxiliary switches are soft commutated.
- QRDCL is phase leg independent. It only takes action on the dc bus of the inverter, so that the number of auxiliary components is fixed in either single phase or three phases applications.
- The power rating of the auxiliary devices is controllable, which can be determined by (2)

III. GENERALIZED THREE-LEVEL QUASI-RESONANT DC-LINK INVERTER

In order to equip a three-phase four-wire multilevel inverter with soft commutated and self voltage balancing abilities, the quasi-resonant dc-link technique is employed and merged with the generalized multilevel inverter. By changing the dc capacitors C_{m1} and C_{m2} into resonant capacitors C_{r1} and C_{r2} . The dc bus of the generalized inverter is transformed into a resonant bus as in Fig. 2(a). Fig. 3 shows the circuit diagram of the proposed generalized three-level quasi-resonant dc-link inverter. Considering the number of extra power devices and their trigger circuits in the system, just one phase leg of the inverter is built by generalized multilevel topology. Another two phase legs are built by traditional diode-clamped structure. The extra inductor L_m is added in order to resist the inrush current when two unbalanced capacitors are connected in parallel.

By keeping the resonant voltage of upper and lower QRDCL modules balanced, switches S_5 or S_6 should not be triggered during the resonant period. If either S_5 or S_6 is turned on during the resonant period, the equivalent resonant capacitance could be changed and results in asynchronous of achieving zero dc-link voltage. Since the generalized multilevel topology inherits the structure of a capacitor-clamped inverter, the capacitor C_m is connected in parallel to the dc bus through two free-wheeling diodes of switches S_1 and S_4 . The energy in the capacitor C_m would transfer to the resonant capacitors C_{r1} and C_{r2} while their voltages are decreased. The resonant voltage would decrease to half of the original value rather than zero. Fortunately, the inductor L_m also acts as a snubber which can snub the energy recharged by capacitor C_m . This shows the fact that quasi-resonant dc-link is not the perfect soft commutated technique in capacitor-clamped inverters, moreover in generalized multilevel inverters. Besides, zero voltage switching would not happen anymore for switches S_2 and S_3 as they are clamped by capacitor C_m .

Control strategy of the overall system will be proposed in the next section and the feasibility of quasi-resonant dc-link generalized three-level inverter will be evaluated by simulation. Key points of combining QRDCL and generalized topology are summarized as follow.

- The inverter is equipped with soft commutated and self voltage balancing abilities.
- Most of the switches are soft commutated except switches S_2 and S_3 .
- Switches S_5 and S_6 are hard switched off since they are switched before the zero voltage condition.
- DC-link voltage would resonant to a small value rather than zero.

IV. CONTROL SYSTEM OF GENERALIZED THREE-LEVEL QUASI-RESONANT DC-LINK INVERTER

A control chart of the generalized three-level quasi-resonant dc-link inverter is shown in Fig. 4. Auxiliary switches S_a is turned on and S_c is turned off when there has

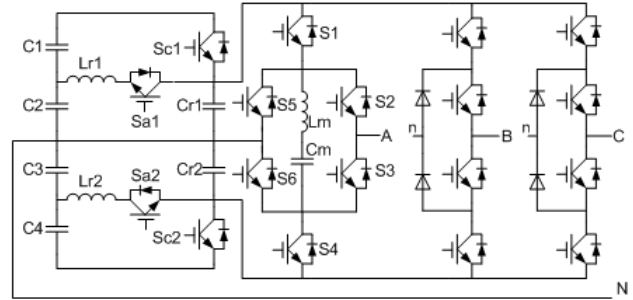


Figure 3. Generalized three-level quasi-resonant dc-link inverter.

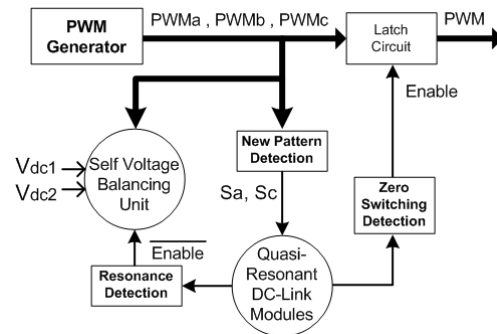


Figure 4. Control diagram of the proposed generalized three-level quasi-resonant dc-link inverter.

changes of the switching pattern of the inverter. S_a will be turned off under zero current switching once the resonant current reaches zero, and S_c is turned on when the resonant voltage is recharged to its original value. The incoming pulse-width modulation (PWM) signals are saved in a latch device, and the signals will be released as soon as the zero voltage condition is detected. A threshold value is selected in the control system for activating the self voltage balancing unit. In addition, conditions of QRDCL modules will feed to the self voltage balancing unit, so that the operations of both balancing unit and QRDCL modules will not be interacted.

V. SIMULATION RESULTS

The generalized three-level quasi-resonant dc-link inverter is evaluated in simulation by using PSCAD/EMTDC. The system is built as a three-phase four-wire voltage supplier and three-phase nonlinear loads are connected to the inverter. The nonlinear currents of the system are shown in Fig. 5. Fig. 6(a) shows the unbalanced dc bus voltages of a traditional inverter and Fig. 6(b) shows the self balanced dc bus voltages of the proposed generalized inverter with QRDCL modules. The figures clearly show that the dc bus voltages are under control in generalized multilevel inverter. Table 2 lists the system parameters of the simulation, and Table 3 gives the estimated switching losses of the generalized multilevel inverter with and without the assistance of QRDCL. It shows that 23.4% of switching losses can be eliminated by employing QRDCL technique without affecting the output performance of the inverter.

TABLE II. SYSTEM PARAMETERS OF SIMULATION

Parameters	Symbols	Value
Nonlinear currents (rms)	la, lb, lc	2.46 A
Neutral current (average)	In	4.7 A
Current frequency	f	50 Hz
DC bus voltage	Vdc	100 V
Resonant inductor	Lr	3 μ H
Resonant capacitor	Cr	0.3 μ F
Balancing inductor	Lm	10 μ H
Balancing capacitor	Cm	200 μ F
Switching frequency	fs	5000 Hz

TABLE III. ESTIMATED SWITCHING LOSSES OF THE INVERTER

Switching Losses without QRDCL applied	Switching losses with QRDCL applied
4.7W	3.6W

VI. CONCLUSION

This paper presents a combination of a generalized multilevel inverter and a quasi-resonant dc-link inverter. Generalized multilevel inverter topology has an attractive ability in balancing the dc bus voltage which is always affected by the zero sequence current in three-phase four-wire power system. The cell structure of the generalized topology enables the inverter to self balance the dc bus voltage without any assists from extra circuits. QRDCL technique is selected in this paper since it has a fixed number of components in either single-phase or three-phase system. The combination of them equips the inverter with self voltage balancing and soft commutated abilities, which can enhance the functionality of a three-phase four-wire inverter. The simulation results show that the proposed generalized three-level QRDCL inverter can control the dc bus voltage and avoid diverging from its desired value. With the assist of quasi-resonant dc-link modules, 23.4% of switching losses can be reduced, hence increasing the efficiency of the proposed generalized three-level quasi-resonant dc-link inverter.

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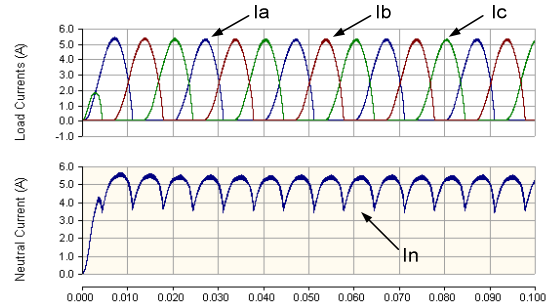
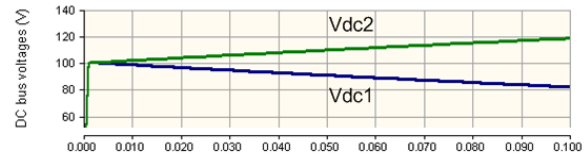
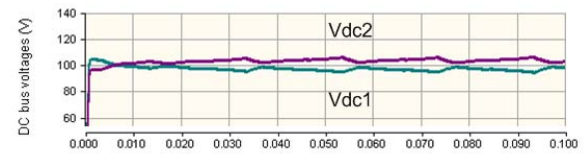


Figure 5. Nonlinear load currents



(a)



(b)

Figure 6. (a) Unbalanced dc bus voltage, (b) balanced dc bus voltage by using proposed inverter.