FPGA-based Decoupled Double Synchronous Reference Frame PLL for Active Power Filters

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***Abstract*—Decoupled double synchronous reference frame Phase-locked loop (DDSRF-PLL) is able to detect the phase angle of positive sequence when the three-phase voltages are unbalanced and distorted. In this paper, it is applied to the compensation current detection algorithm of shunt active power filter (SAPF) to replace a conventional PLL. Simulation results indicate that the compensation performance could be improved under voltage unbalance and distortion. Besides, DDSRF-PLL implemented on one field-programmable gate array (FPGA) chip is proposed. When compared with widely used digital signal processors (DSPs) in power control, FPGA the proposed structure has the advantages of parallel processing and rich user-defined I/O ports so that it exhibits processing efficiency and flexibility in application.**

Keywords-Decoupled double synchronous reference frame Phase-locked loop (DDSRF-PLL); shunt active power filter (SAPF); field-programmable gate array (FPGA)

I. INTRODUCTION

In Three-Phase systems PLLs can be adopted in the compensation current detection algorithm of shunt active power filter (SAPF) [1]-[3] if the instantaneous phase angle of positive sequence is wanted. Without considering harmonics in source voltages, the phase A is always in phase with the α component of Three-Phase source voltages. And, when these are balanced, the α component will be in phase with the positive sequence. In conventional three-phase PLLs [4]-[6] and single-phase PLLs [7]-[9], the phase-lock is believed to be in phase with that α component. However, the α component will not be in phase with the positive sequence when the source voltages are unbalanced. In order to guarantee that the detected results are accurate conventional PLLs should be replaced.

This work proves that the DDSRF-PLL [10][11] can be applied in the compensation current detection algorithm of SAPF in the unbalanced case and it introduces its implementation on a FPGA chip. DSP is widely utilized as the control device in traditional power systems [12][13], but its processing efficiency is limited by small capability and flexibility. The proposed FPGA-based DDSRF-PLL exhibits the advantages of a FPGA system, which can realize parallel processing for efficiency improvement, and enhancement of connectivity through the rich user-defined I/O ports between sub-systems. Furthermore, the FPGA-based system can be further developed as an application specific integrated circuit (ASIC) to be embedded in the control system of different applications. In this paper, the operation principles of compensation current detection algorithm and DDSRF-PLL are introduced in section Ⅱ. In order to verify the influence of DDSRF-PLL and conventional PLL in compensation, corresponding simulation results are provided in section Ⅲ. The implementation of DDSRF-PLL on FPGA is discussed in section Ⅳ. Experimental verification will be given in section Ⅴ.

II. OPERATION PRINCIPLES

The typical compensation current detection algorithm using PLL is SRF method. And SRF-PLL is adopted. However, such conventional PLL is not applicable in unbalanced case. SRF method could be used in both balanced and unbalanced cases if only conventional PLL is replaced by DDSRF-PLL.

A. SRF method

The block of SRF method is shown in Fig. 1. Load currents in dq reference frame are calculated by

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = [C][T_{dq}] \begin{bmatrix} i_{la} \\ i_{lb} \\ i_{lc} \end{bmatrix}. \tag{1}$$

Where

$$[C] = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}, \tag{2}$$

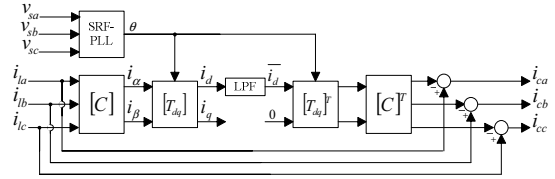


Figure 1. Block diagram of SRF method with SRF-PLL

$$[T_{dq}]=\begin{bmatrix} cos(\theta) & sin(\theta) \\ -sin(\theta) & cos(\theta) \end{bmatrix}. \quad (3)$$

The positive-sequence components of load currents are changed into the dc components of i_d and i_q. The rest components, such as negative sequence and harmonics, are transformed to the ac components of i_d and i_q. When this compensation current detection algorithm provides a full compensation, only the dc component of i_d should be held. And the dc component is extracted by a low-pass filter (LPF). Thus, the compensation currents are obtained by

$$\begin{bmatrix} i_{ca} \\ i_{cb} \\ i_{cc} \end{bmatrix}=\begin{bmatrix} i_{la} \\ i_{lb} \\ i_{lc} \end{bmatrix}-[C]^T[T_{dq}]^T\begin{bmatrix} \bar{i}_d \\ 0 \end{bmatrix}. \quad (4)$$

Based on (1) and (4), the detected compensation currents would be accurate as soon as the instantaneous phase angle in the transformation matrixes is in phase with positive sequence. In other words, the precision of this compensation current detection algorithm is determined by the PLL.

B. DDSRF-PLL

The expression of the fundamental voltage vector on the αβ reference frame is defined as

$$\begin{aligned} \boldsymbol{v}_{s(\alpha\beta)} &= \begin{bmatrix} v_{s\alpha} \\ v_{s\beta} \end{bmatrix} = \boldsymbol{v}_{s(\alpha\beta)+1} + \boldsymbol{v}_{s(\alpha\beta)-1} \\ &= V_{s+1}\begin{bmatrix} cos(\omega t) \\ sin(\omega t) \end{bmatrix} + V_{s-1}\begin{bmatrix} cos(-\omega t+\varphi_{-1}) \\ sin(-\omega t+\varphi_{-1}) \end{bmatrix}. \end{aligned} \quad (5)$$

The superscript +1 and -1 define coefficients of the positive and negative sequence components, respectively. The voltage vector in αβ reference frame consists of two sub-vectors: V_{s+1}, rotating with a positive angular frequency ω, and V_{s-1}, rotating with a negative angular frequency –ω.

The double SRF is composed of two rotating reference frames: dq+1, rotating with the positive direction and whose angular positive is θ′, and dq-1, rotating with the negative direction and whose angular positive is -θ′. The block diagram of DDSRF-PLL is shown in Fig. 2. If the vector in αβ reference frame is expressed in the double SRF, (6) and (7) are obtained.

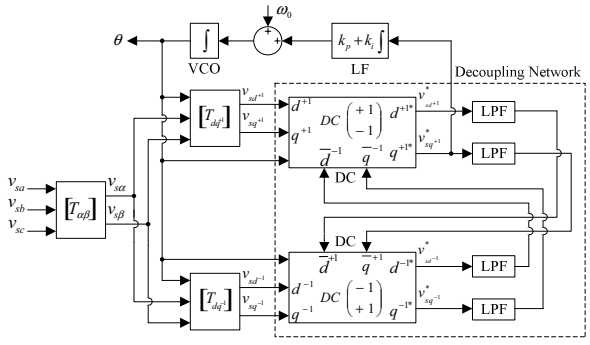


Figure 2. Block diagram of DDSRF-PLL

$$\begin{aligned} \boldsymbol{v}_{s(dq^{+1})} &= \begin{bmatrix} v_{sd^{+1}} \\ v_{sq^{+1}} \end{bmatrix} = [T_{dq^{+1}}]\boldsymbol{v}_{s(\alpha\beta)} \\ &= V_{s+1}\begin{bmatrix} cos(\omega t-\theta') \\ sin(\omega t-\theta') \end{bmatrix} + V_{s-1}\begin{bmatrix} cos(-\omega t+\varphi_{-1}-\theta') \\ sin(-\omega t+\varphi_{-1}-\theta') \end{bmatrix}, \end{aligned} \quad (6)$$

$$\begin{aligned} \boldsymbol{v}_{s(dq^{-1})} &= \begin{bmatrix} v_{sd^{-1}} \\ v_{sq^{-1}} \end{bmatrix} = [T_{dq^{-1}}]\boldsymbol{v}_{s(\alpha\beta)} \\ &= V_{s+1}\begin{bmatrix} cos(\omega t+\theta') \\ sin(\omega t+\theta') \end{bmatrix} + V_{s-1}\begin{bmatrix} cos(-\omega t+\varphi_{-1}+\theta') \\ sin(-\omega t+\varphi_{-1}+\theta') \end{bmatrix}, \end{aligned} \quad (7)$$

$$[T_{dq^{+1}}]=[T_{dq^{-1}}]=\begin{bmatrix} cos(\theta') & sin(\theta') \\ -sin(\theta') & cos(\theta') \end{bmatrix}. \quad (8)$$

The harmonics in source voltages could be restrained by PLL. Based on the small signal analysis, θ′ is believed to be equal to the phase ωt when the phase is locked. Equations (6) and (7) should be rewritten as (9) and (10), respectively. And the q component in (9) should be equal to zero as conventional ones if the oscillation with 2ω frequency is not included.

$$\boldsymbol{v}_{s(dq^{+1})} = V_{s+1}\begin{bmatrix} 1 \\ \omega t-\theta' \end{bmatrix} + V_{s-1}\begin{bmatrix} cos(-2\omega t+\varphi_{-1}) \\ sin(-2\omega t+\varphi_{-1}) \end{bmatrix}, \quad (9)$$

$$\boldsymbol{v}_{s(dq^{-1})} = V_{s+1}\begin{bmatrix} cos(2\omega t) \\ sin(2\omega t) \end{bmatrix} + V_{s-1}\begin{bmatrix} cos(\varphi_{-1}) \\ sin(\varphi_{-1}) \end{bmatrix}. \quad (10)$$

And decoupling network is adopted to cancel the oscillations with 2ω frequency and improve dynamic response. Detailed introduction to the DC is given in [10][11].

III. APPLICATION OF CONVENITIONAL SRF-PLL AND DDDSRF-PLL IN THREE-PHASE FOUR-WIRE SAPF

A three-phase four-wire compensation system, shown in Fig. 3, is simulated by using PSCAD/EMTDC. The main circuit of the SAPF is a two-level four-leg voltage source inverter (VSI). Its control system, shown in Fig. 4, consists of 4 parts. The compensation current detection algorithm is SRF method. Calculation of reference voltages in [14] and 3D direct PWM method in [15] are adopted in the control system. In order to test the compensation performance, SRF-PLL and DDSRF-PLL are used in the compensation current detection algorithm, respectively.

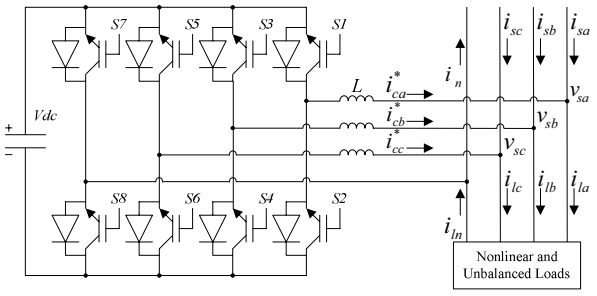


Figure 3. Three-phase four-wire compensation system

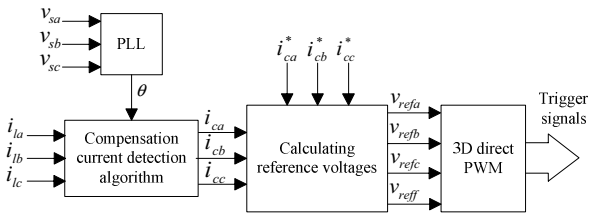


Figure 4. Block diagram of control system in SAPF

The waveforms of three-phase source voltages in the compensation system are given in Fig. 5. They are unbalanced and contain harmonics. And the loads are nonlinear and unbalanced. The waveforms of load currents are shown in Fig. 6. Corresponding power factor (PF), total harmonic distortion (THD) and root mean square (RMS) value of neutral current are listed in Table Ⅰ. If the SAPF does not provide compensation to the system, the source currents would be the same as the load currents. Reactive current, current harmonics and neutral current is necessary to be compensated. When SRF-PLL and DDSRF-PLL are respectively adopted and the SAPF provides full compensation, the waveforms of compensated source currents are exhibited in Figs. 7 and 8. Corresponding parameters of source currents, such as PF, THD and RMS value of neutral current after compensation are also listed in Table Ⅰ.

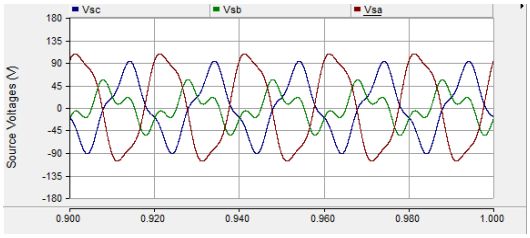


Figure 5. Source voltages

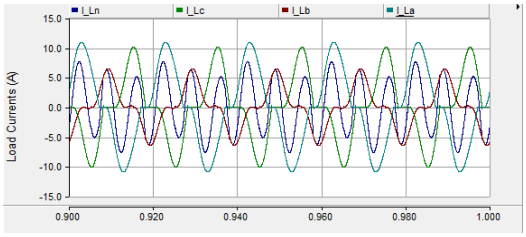


Figure 6. Load currents

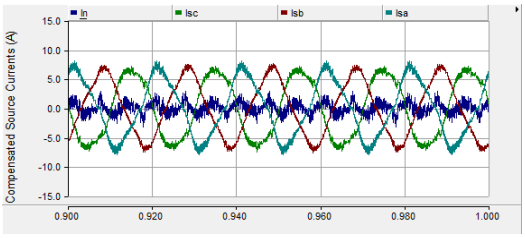


Figure 7. Compensated source currents using conventional SRF-PLL

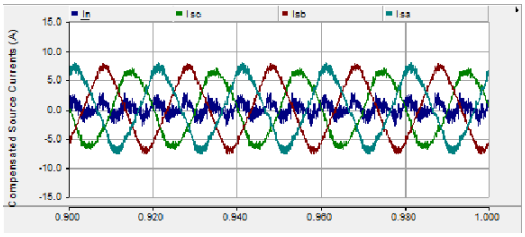


Figure 8. Compensated source currents using DDSRF-PLL

TABLE I. SIMULATION RESULTS

		Load Currents	Source Currents	
			SRF-PLL	*DDSRF-PLL*
PF	***A***	0.903	0.997	0.999
	B	0.952	0.999	0.999
	C	0.999	0.999	0.999
THD	***A***	25.45%	14.30%	8.68%
	B	43.67%	10.63%	7.60%
	C	42.70%	10.25%	7.22%
Neutral		4.7A	0.9A	1.0A

The simulation results in Table Ⅰ indicate reactive current, currents harmonics and neutral current are compensated. And the comparison between SRF-PLL and DDSRF-PLL proves the analysis in previous section. DDSRF-PLL could provide accurate phase of positive sequence so that the SAPF could provide accurate compensation in unbalanced case. Therefore, DDSRF-PLL is more advisable than conventional one in improving source currents.

IV. DDSRF-PLL IMPLEMENTATION

The chip selected is XC3SD1800A-4FGG676C Spartan-3A DSP FPGA which is provided by XILINX Company. It contains rich hardware resource and clock source. In the designed digital system, sampling frequency is 5 KHz while global clock is 125 MHz. And there are 4 main blocks which are discussed in the following sections. They are LPFs, loop filter (LF), voltage-controlled oscillator (VCO) and look-up table (LUT).

A. LPFs

The LPFs are included in the decoupling network to extract dc components. In order to keep all the outputs of the LPFs be synchronized, the 4 LPFs are identical each other. And the coefficients of the LPFs are obtained by Filter Design &Analysis Tool in MATLAB.

The harmonics in power system are determined by the odd-order components. The characteristic results in harmonics, which should be restrained by the LPFs, are the components with the angular frequencies such as 2ω, 4ω, 6ω and so on. Furthermore, it is necessary to make a compromise between dynamic response and attention of the LPF. Therefore, first-

order LPF which cut-off frequency is 40Hz is adopted for the all digital system. And butterworth infinite impulse response (IIR) LPF is chosen in the design. The transfer function of the designed LPF is given as

$$H(z)=\frac{0.0245+0.0245z^{-1}}{1-0.9510z^{-1}}. \quad (11)$$

The step response shown in Fig. 9 indicates designed LPF has good dynamic response. The coefficients in (11) would be expressed by 16 bits and Q15 format in digital system.

B. LF

The LF is a proportion integral control. And the two processing are parallel. The integral operation is emphasized herein. In discrete system, it is approximated by

$$Tz/(z-1). \quad (12)$$

T is the sampled period 0.0002s. And this integral operation is implemented by an adder, a multiplier and a register as shown in Fig. 10.

In LF, the constants K_i and K_p have a relationship for optimum transient response in conventional SRF-PLL as

$$\xi = 0.5K_p/\sqrt{K_i} \approx 0.707. \quad (13)$$

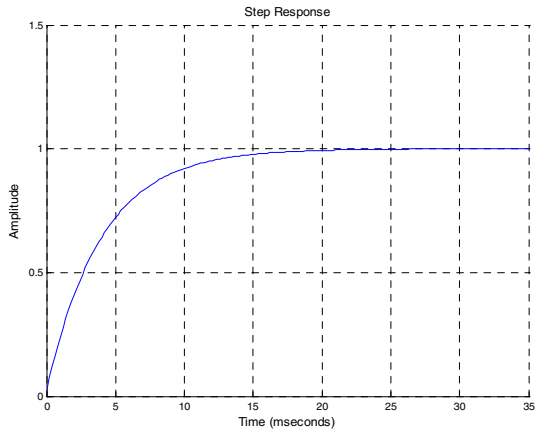


Figure 9. Step response of designed LPF

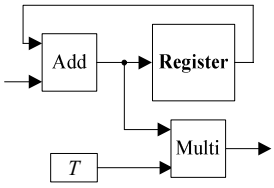


Figure 10. Block diagram of integral operation

Low Ki would improve the performance of noise rejection, but dynamic response would be weakened [16]. And this characteristic is also applicable in DDSRF-PLL. Constants Ki= $(35\pi)^2$ and Kp=1.414×35π are chosen for the PLL system. Fig. 11 shows the bit width and format defined in the LF. Since enough bit width is provided, overflow does not occur.

C. VCO

VCO is also an integral operation, essentially. However, the bit width is finite. If the integral operation in VCO is not modified, overflow must occur. Considering the VCO's output is phase angle, it is periodic which period is 2π. This characteristic could be applied in the modification. The integral operation in VCO should be reset as soon as its output larger than or equal to 2π. A comparison processing should be added. Thus, VCO's output would be periodic. The detailed block diagram of modified integral operation is given in Fig. 12. Corresponding bit width and format could also be read directly.

D. LUT

LUT is usually adopted in digital system to retrieve the closet sine or cosine value from a memory address. Sine or cosine value is stored in a ROM beforehand. In all digital PLL system, the VCO's output is the phase angle. The PLL's outputs are corresponding sine and cosine values rather than the phase angle. The VCO provides instantaneous phase to the LUT. Then, the LUT generates corresponding sine and cosine values.

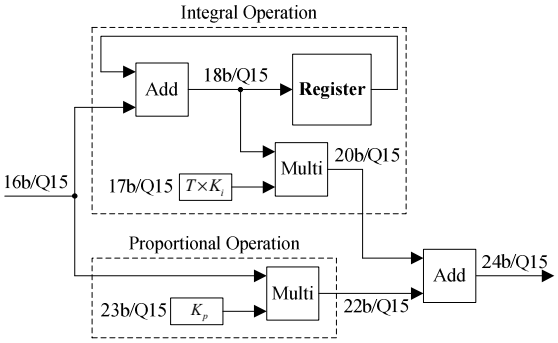


Figure 11. Block diagram of LF

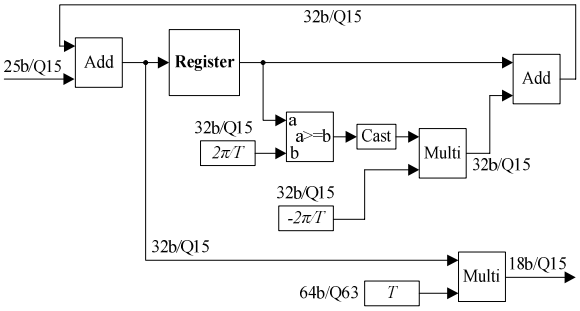


Figure 12. Block diagram of modified integral operation in VCO

If a LUT has n bits address, there are 2^n points in one period 0.02s. The difficulty is how to associate instantaneous phase angle θ with the LUT's address. For the m points LUT, the range [0, 2π) is distributed into m areas with same width. So each width is 2π/m. The first area is in the range [0, 2π/m), the second area is in the range [2π/m, 4π/m) and so on. The area on which the instantaneous phase angle θ is located is associated with corresponding sine or cosine value. For instance, the instantaneous phase angle θ is located on the pth area if the integer part of mθ/2π is equal to p. In the designed system, the sine or cosine LUT has 128 points. And the values are expressed by 16 bits and Q15 format.

V. EXPERIMENTAL VERIFICATION

XtremeDSP Starter Platform – Spartan-3A DSP 1800A Edition is the target FPGA board in experiment while Agilent 16801A Logic Analyzer is used for checking the design. The device utility summary of XC3SD1800A-4FGG676C Spartan-3A DSP FPGA is listed in Table Ⅱ.

In order to prove the FPGA-based DDSRF-PLL is applicable in unbalanced case, positive, negative and zero sequences are given as

$$v_+ = 0.6\sin(100\pi t + \pi/3), \tag{14}$$

$$v_- = 0.07\sin(100\pi t + \pi/4), \tag{15}$$

$$v_0 = 0.02\sin(100\pi t + \pi/8). \tag{16}$$

Thus, the amplitude of fundamental voltage in each phase is different while the phase difference is not strictly equal to 2π/3 or -2π/3.

Furthermore, the capability to restrain harmonics should also be proved. There is a characteristic of the harmonics in power system that even-order components can be ignored and harmonics are determined by odd-order components. Third-order harmonic component added in each phase to simulate harmonic components. They are given as

$$v_{sa\_h} = 0.1\sin(300\pi t + \pi/2), \tag{17}$$

$$v_{sb\_h} = 0.1\sin(300\pi t + \pi/5), \tag{18}$$

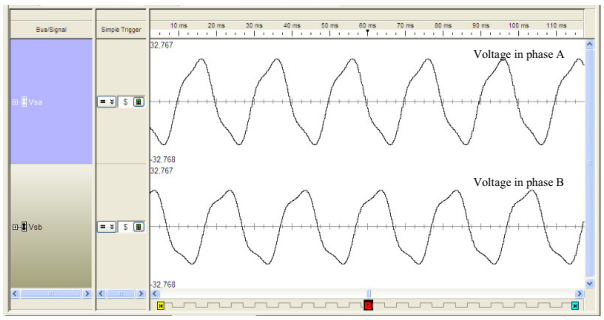
TABLE II. DEVICE UTILITY SUMMARY

Logic Utilization	Used	Available
Number of Slice Flip Flops	3815	33280
Number of 4 input LUTs	4475	33280
Number of occupied Slices	2845	16640
Number of bonded IOBs	83	519
Number of BUFGMUXs	1	24
Number of DSP48As	25	84
Number of RAMB16BWERs	2	84

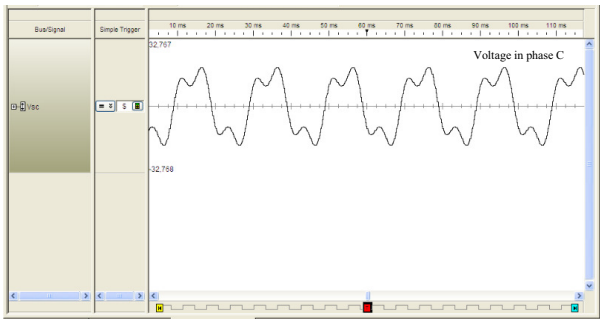
$$v_{sc\_h} = 0.2\sin(300\pi t + \pi/5). \tag{19}$$

The input signals simulating unbalance source voltages with harmonics are expressed by 16 bits and Q15 format. They are stored in ROMs of FPGA beforehand. Fig. 13 shows the experimental results of the input signals. The input signals are unbalanced and not sinusoidal. Since the data captured by Agilent 16801A Logic Analyzer is expressed by 16-bit signed integer, the maximum and minimum values of ordinate in Fig. 13 are 32767 and -32768, respectively. The experimental results are right, although the simulation results of input signals are not provided herein.

In the designed DDSRF-PLL system, it can generate sine and cosine values with unit amplitude and should be in phase with positive sequence. Both the outputs are expressed by 16 bits and Q15 format. In hardware verification, sine wave with unit amplitude which is in phase with positive sequence is stored in a ROM of FPGA beforehand. It is used as the ideal output and expressed by 16 bits and Q15 format. The sine value generated by DDSRF-PLL is compared with it in Fig. 14. The data in Figs. 14 and 15 is also expressed by 16-bit signed integer, so the maximum and minimum values of ordinate are 32767 and -32768, respectively. Fig. 14 shows DDSRF-PLL begin to work at M. And it verifies DDSRF-PLL can track the phase of positive sequence. Fig. 15 shows the error between ideal output and DDSRF-PLL output. DDSRF-PLL begins to work at M1 and reach steady state at M2. It indicates DDSRF-PLL spends 0.03 s in locking the phase of positive sequence. During steady state, the maximum fluctuation of the error is about 655.



(a)



(b)

Figure 13. Experimental results of input signals (a) Source voltages in phase A and phase B (b) Source voltage in phase C

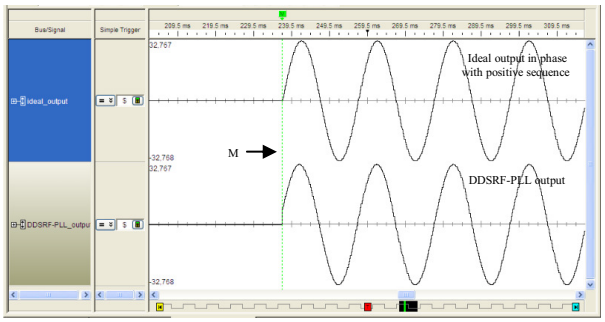


Figure 14. Experimental results of ideal sine wave and actual sine wave

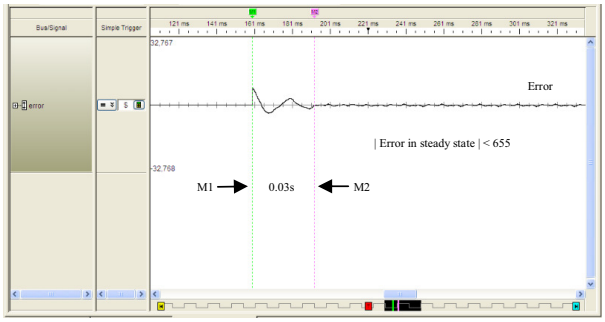


Figure 15. Experimental result of error between ideal sine wave and actual sine wave

Without considering device utility, FPGA-based DDSRF-PLL can provide more accurate results if only the data in FPGA is expressed by longer bit width and store more points in LUT. The reason is that the frequency of global clock is very high so that the FPGA has high processing efficiency. In addition, the tracking time would still be 0.03s under the same input signals as Fig. 13.

VI. CONCLUSIONS

DDSRF-PLL overcomes the limitations of conventional PLLs and it can be used for compensation of the current detection algorithm of SAPFs, in either balanced or unbalanced modes. In this paper, the all digital DDSRF-PLL has been implemented on XC3SD1800A-4FGG676C Spartan-3A DSP FPGA, with important parameters discussed and provided, as well as with the introduction of the appropriate strategies to solve the main problems. The experimental results prove that the all digital PLL system can provide accurate phase of the positive sequence. Besides these, the FPGA-based system presents many advantages, such as high processing efficiency, flexible user-defined I/O ports and validation for ASIC. Therefore, it is advisable to utilize such type of FPGA implementation.

ACKNOWLEDGMENT

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