Hardware Realization of a 10KVA Hybrid Active Power Filter

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***Abstract*—This paper presents a hardware realization of a *LC* coupled hybrid active power filter (*LC*-HAPF). According to the characteristics of the load, the corresponding passive part of the *LC*-HAPF and the reference dc-link voltage can be designed, under the requirement of IGBT and the digital signal processor (DSP), the IGBT driver and the signal condition board for the DSP can be designed too. Finally, based on the design, the compensation control algorithm for the *LC*-HAPF can be implemented by the DSP, and all the compensation results satisfied the international standars.**

Keywords-LC-HAPF; passive part; reference dc-link voltage; IGBT driver; signal conditon board

I. INTRODUCTION

According to the development of science and technology, power electronics equipments (nonlinear loads) such as converters, adjustable speed drives (ASDs), arc furnaces, bulk rectifiers, TV sets, power supplies etc. are more and more used in utility power system. As a result, a lot of solid state power converters such as thyristors rectifiers and cycloconverters are used. The main consequence of the great increasing of those devices used in the electric network is that the current and voltage signals in the electric network are serious distorted, so the problems of current harmonic and power factor are significant. These power quality problems may affect the safety operation and increase the loss of the power grid and electrical equipments [1]-[3].

In order to solve those power quality problems, power quality filters are widely used. Passive filters (PFs) have been broadly used to suppress harmonics and improve power factor due to their low cost, simplicity and high efficiency, and usually connected parallel with the load. However, it has some drawbacks such as resonance problems, low dynamic response, dependent filtering characteristics, etc. [4]-[5]. To overcome the disadvantages inherent in PFs, active power filters (APFs) have been developed, but the initial costs and running costs of the APFs are much higher than PFs [6]-[7]. In order to combine the advantages of both PFs and APFs, hybrid active power filters (HAPFs) which consist of active and passive filters connected in series or parallel with each other have been constructed. The main purpose of the HAPFs is to reduce initial costs and to improve efficiency. It leads to the best effectiveness in cost and performance [8]-[9].

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Among the existing HAPF topologies, since the LC coupled hybrid active power filter (*LC*-HAPF) [10] contains only a few passive components and the dc-link operation voltage can be much lower than the APF, the *LC*-HAPF topology is chosen in this paper.

For the *LC*-HAPF, an appropriate design of passive part and reference dc-link voltage can improve the system compensation performance and reduce the initial cost, therefore the design criteria of the coupling inductor L_c, coupling inductor C_c and the reference dc-link voltage V_{dc} are important factors. Moreover, to make sure the system works properly, an appropriate input signal for the DSP and the IGBT to implement the control algorithm and drive the IGBT respectively should be properly designed.

In this paper, the design of the *LC*-HAPF passive part and the reference dc-link voltage are introduced at first, and then the design of the IGBT driver and the signal condition board will be given. Finally, the hardware construction and hardware results based on those design will be illustrated to verify its current quality compensation capability.

II. DESIGN OF A THREE-PHASE FOUR-WIRE *LC*-HAPF

A. Design of LC-HAPF passive part

When there is large number of single-phase loads, serious neutral current, harmonic and reactive power burden, and three-phase unbalance will be caused in the system. To reduce these problems, a three-phase four-wire *LC*-HAPF can be implemented. Figure 1 and Figure 2 show the two typical configurations of three-phase four-wire *LC*-HAPF.

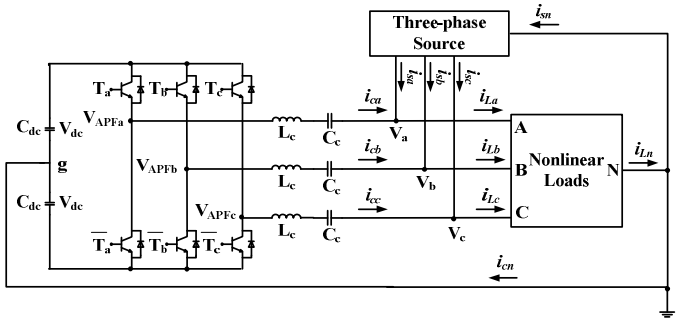


Figure 1. A three-phase four-wire center-split *LC*-HAPF

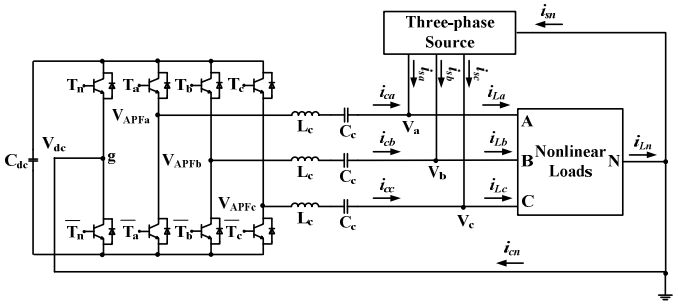


Figure 2. A three-phase four-wire four-leg *LC*-HAPF

The first configuration as shown in Figure 1 is a three-phase four-wire center-split *LC*-HAPF, the second configuration as shown in Figure 2 is a three-phase four-wire four-leg *LC*-HAPF. The three-phase four-wire four-leg *LC*-HAPF can give a good neutral line current compensation by its fourth leg [11]-[12]. However the extra fourth leg increases its initial cost, therefore, the three-phase four-wire center-split *LC*-HAPF is widely chosen.

The passive part of the *LC*-HAPF is used to compensate the reactive power and harmonic current, so that the capacity of the active part can be reduced. The design of the L_c and C_c value should be determined according to the nonlinear load. The capacitor C_c is used to compensate the reactive power and the capacitor C_c and inductor L_c in series is used to compensate the harmonic current. Therefore, the design for the coupling capacitor and inductor can be expressed as follow.

$$C_c = \frac{V_x^2}{2\pi f \cdot Q_x} \tag{1}$$

$$L_c = \frac{1}{(n \cdot 2\pi f)^2 \cdot C_c} \tag{2}$$

In (1) and (2), f is the current fundamental frequency which is 50Hz, V_x represents the phase source voltage, Q_x represents the reactive power generated by the load, n means the order of harmonic current. Both V_x and Q_x can be measured by the power measuring instruments before designing the passive part of the *LC*-HAPF. The coupling capacitor C_c should be determined by (1) first, and then the coupling inductor L_c should be determined by (2). The order of the harmonic current cannot be turned at a small value (eg. the third harmonic), because the required large L_c value makes the size of the *LC*-HAPF huge and increase the initial cost.

B. Design of dc-link reference voltage

A stable dc-link voltage is the guarantee of a good power quality compensation performance for the *LC*-HAPF. However a low dc-link voltage cannot give a strong support to the *LC*-HAPF system and the compensation result is not good, a high dc-link voltage will make big noise and the compensation result becomes bad. Moreover the high dc-link voltage will increase the initial cost of the *LC*-HAPF system, therefore a suitable dc-link voltage is necessary.

By reference [13], the required output voltage of the active inverter part of the *LC*-HAPF can be present as follow:

$$V_{APF} = \sqrt{\left|V_{APFf}\right|^2 + \sum_{n=2}^{\infty}\left|V_{APFn}\right|^2} \tag{3}$$

$$V_{APFf} = V_x - \left|X_{LCf} - X_{CCf}\right|\left|I_{Cfq}\right| \tag{4}$$

$$V_{APFn} = \left|X_{LCn} - X_{CCn}\right|\left|I_{Cn}\right| \tag{5}$$

In (3), (4) and (5), V_{APFf} is the required active inverter fundamental output voltage, V_{APFn} is the active inverter required harmonic output voltage at each nth harmonic order. V_s is the root-mean square (rms) phase-to-phase source voltage, I_{Cfq} is the compensation rms current at fundamental frequency, I_{Cn} is the compensation rms current at nth order harmonic frequency, X_{LCf} and X_{CCf} are the impedances of the coupling inductor and capacitor at fundamental frequency, X_{LCn} and X_{CCn} are the impedances of the coupling inductor and capacitor at nth order frequency. Based on full compensation situation, the compensation currents should be equaled to the load reactive and harmonic currents. Due to the impedance of the inductor and capacitor is known, therefore, the V_{APFf} and V_{APFn} can be calculated via (4)-(5).

$$\begin{aligned}\left|I_{cfq}\right| &= \left|I_{Lfq}\right| \\ \left|I_{cn}\right| &= \left|I_{Ln}\right|\end{aligned} \tag{6}$$

After getting V_{APFf} and V_{APFn}, the minimum required dc-link voltage V_{dc_HAPF} for the three-phase four-wire *LC*-HAPF is:

$$V_{dc\_HAPF} = \frac{\sqrt{2}}{m} V_{APF} \tag{7}$$

In (7) m is the modulation index. Since m is smaller than 1 during under-modulation case, therefore, the minimum dc-link voltage for the three-phase four-wire center-split *LC*-HAPF can be written as:

$$V_{dc} = V_{dc\_HAPF} = \sqrt{2} V_{APF} \tag{8}$$

C. Design of IGBT driver

Due to the IGBT has the merit of low switching losses and require very little drive power at the gate, the IGBT is now beginning to have a major impact on the power electronic systems in the low to medium power range, in this experiment

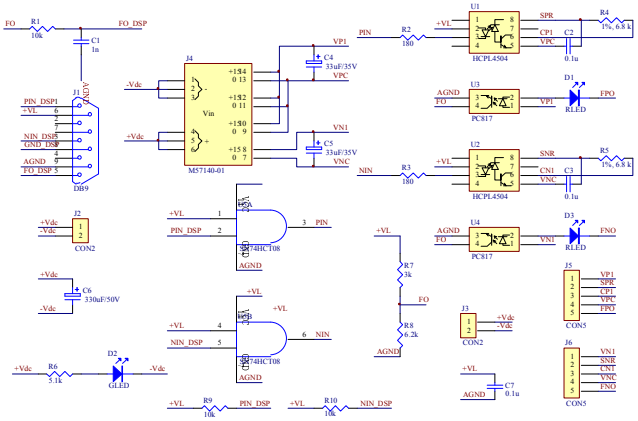


Figure 3. Schematic of the IGBT driver for PM300DSA60

system, the Mitsubishi third generation IGBT PM300DSA60 which maximum rated current and voltage are 300A and 600V respectively is selected as the switching device. In order to control the switching state of IGBT with the trigger signals from digital controller, an IGBT driver is necessary. Figure 3 shows the schematic of the IGBT driver for PM300DSA60.

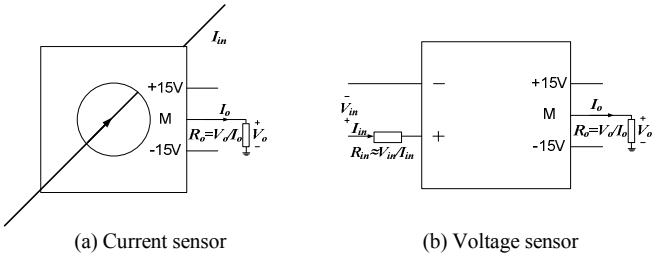
In Figure 3, Port DB9 is for the input signal and Port CON5 is for the output signal. M57140-01 is an isolate DC-to-DC converter designed to drive the intelligent power modules (PM300DSA60). The followings are some considerations for the design of the IGBT driver in consideration of controller I/O requirement.

1. The SN74HCT08 is used to protect the I/O of DSP controller. It works as a buffer since the current of the I/O is recommended to within 1.67mA per pin for 3.3 V-tolerance; while the typical working current of HCPL4504 is 16mA.
2. +VL, R7 and R8 are combined as resistor divider to pull up the signal "FO" and limit the voltage within 3.3V.
3. The RC low-pass filter is adopted to filter the noise which could probably be on the fault signal. The selection of R1 should consider the current of controller I/O, "FO" pull up potential and RC low-pass filter's loading effect.

D. Design of the signal condition board

For a 10KVA system, when the system source voltage is defined as 220V, the current in each phase cannot exceed 15A, therefore, in this paper, the selection and design of all the components will be based on this voltage and current standards.

In order to get the necessary parameters from the system to the DSP to implement the control algorithm, a signal condition board is essential, the signal condition board includes voltage sensor, current sensor and their corresponding signal condition circuit. Figure 4 shows the configuration of the current and voltage sensor.



(a) Current sensor (b) Voltage sensor

Figure 4. Configration of current and voltage sensor

To select a suitable current sensor depends on the load current, in this experiment system, the maximum load current is less than 20A, therefore current sensor KT20A/P is selected, the parameters of KT20A/P are shown in TABLE 1.

TABLE 1. PARAMETERS OF CURRENT SENSOR KT 20A/P

Type	Measurement current	Output current	Linearity
KT 20A/P	20A	100mA	≤0.2%

The voltage sensor is used to get the voltage parameters from the source and the dc-link, in this experiment system, the peak value of the source voltage is about 330V, the maximum dc-link voltage is about 200V, thus voltage sensor KV 50A/P is selected and its parameters are shown in TABLE 2.

TABLE 2. PARAMETERS OF CURRENT SENSOR KV 50A/P

Type	Primary side current	Output current	Linearity	Measurement range
KV 50A/P	10mA	50mA	≤0.2%	1000V

To get the best measurement results from TABLE 2, the primary side current should get close to the rate current 10mA, therefore, the input series resistor R_{in} for the source voltage measurement R_{in_source} and dc-link voltage measurement R_{in_DC} should be:

$$R_{in\_source} = 330/0.01 = 33k\Omega$$
$$R_{in\_DC} = 200/0.01 = 20k\Omega \quad (9)$$

All the measurements from the sensors are sent to the DSP to perform the calculations, however, different signal levels from the sensors are not compatible with DSP. Therefore, a signal condition circuit is needed to provide appropriate and synchronies signal levels. Figure 5 shows the schematic of the signal condition circuit.

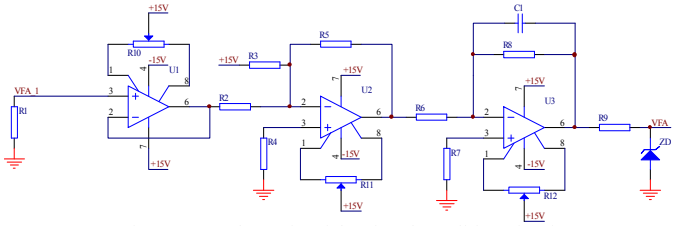


Figure 5. Schematic of the signal condition circuit

From Figure 5, the signal condition board is constructed by one voltage follower and two negative gain amplifiers. The voltage follower provides high input impedance to avoid loading effect, while the two negative gain amplifiers provide a suitable and positive output signal to DSP. There is a Zener diode is installed at the output side to limit the output within the acceptable range, a 3.3V Zener diode is used for the 3.3V DSP. This design can protect the control unit when over output situation.

The resistor R_1 is the series output resistor R_o in the current sensor and the voltage sensor shown in Figure 4, therefore, the output voltage of the current and voltage sensor V_o is the input voltage of the signal condition circuit *VFA_1*. In order to synthesize the parameters of the signal condition circuit, the R_1 for the current sensor KT20A/P is selected as 50Ω, while that of voltage sensor KA50A/P is selected as 100Ω. Due to the rated output current of KT20A/P is 100mA, the rated output current of the KA50A/P is 50mA, thus the input voltage for both current sensor signal condition board and voltage sensor signal condition board is the same 5V(rms), the peak value of the input voltage value is 5√2V.

A digital signal processor TMS320F2812 is chosen as the control system of the *LC*-HAPF and its maximum input voltage is 3.3V, thus, the peak output voltage from the signal condition circuit should be consistent with the input voltage of DSP. In

order to avoid the unsteady state of the DSP when the input voltage of the DSP approaches 3.3V, the peak output voltage is changed and consistent with 0-3.0V of DSP. According to the schematic shown in Figure 5, the input-output relation of the signal condition board can be described as the following equation:

$$V_O = (R_5 / R_2) \cdot V_{in} + (R_5 / R_3) \cdot 15 \qquad (10)$$

where V_o is the output voltage, VFA in Figure 5 is the output voltage V_o, V_{in} is the input voltage, VFA_1 in Figure 5 is the input voltage V_{in}.

Because the input signal for the DSP is positive, therefore for an ac measurement, a dc offset is necessary and the offset value is depended on the suitable input range of the control unit. In this experiment, the range of DSP input signal is 0-3.0V, thus a dc offset of 1.6V is necessary, from Figure 5, the dc offset V_{dc_offset} is controlled as following.

$$V_{dc\_offset} = (R_5 / R_2) \cdot 15 \qquad (11)$$

where the dc offset can be changed by adjusting the ratio of R_5 and R_2.

According to (10)-(11), select R_5=2.2KΩ, R_3=20KΩ, R_2=8.2KΩ, R_4=1.5KΩ, R_6=R_8=10KΩ, R_7=5KΩ. R_{10}, R_{11}, R_{12} are 20KΩ adjustable resistor.

Finally, R_8 and C_1 combine as an active first order low-pass filter, which aims at filtering the high frequency noise signal existed in the digital system. The determination of C_1 parameter refers to the filter design.

III. HARDWARE RESULTS

Figure 6 and Figure 7 show the overall configuration and the experimental prototype of the *LC*-HAPF.

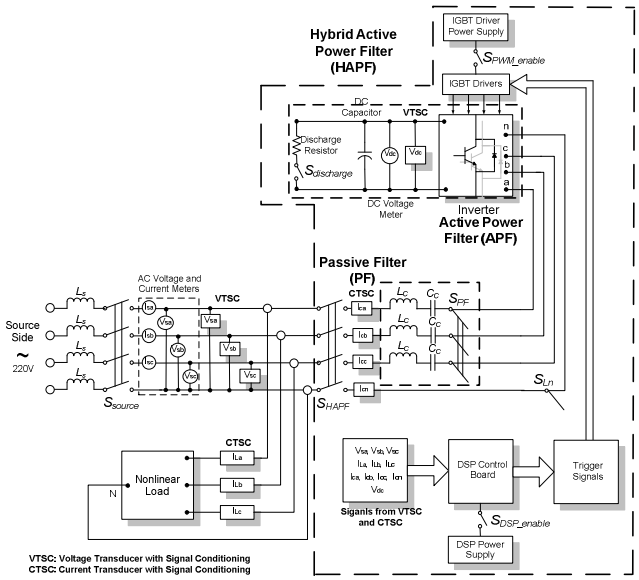
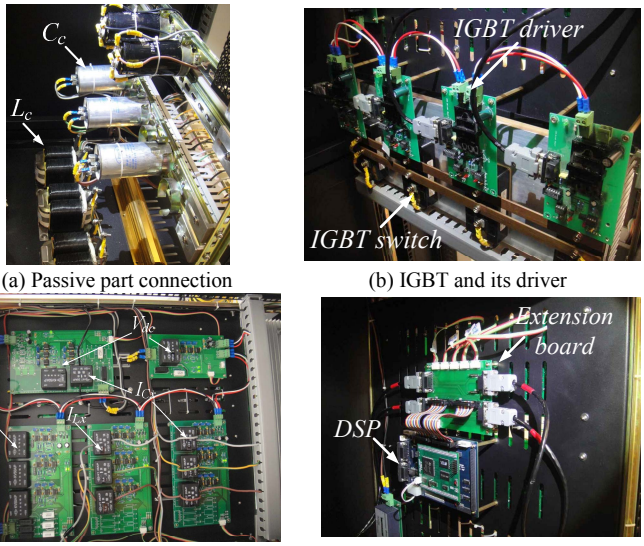


Figure 6. Overall system configuration of the experimental *LC*-HAPF system

Figure 7. Experimental prototype of the *LC*-HAPF

From Figure 6, six current sensor circuits and five voltage sensor circuits are used for detecting three load currents, three compensation currents, three source voltages and two dc-link voltages respectively. Figure 6 also indicates the connection of the IGBT driver and the DSP. Figure 8 shows the photo of different parts of the *LC*-HAPF system.



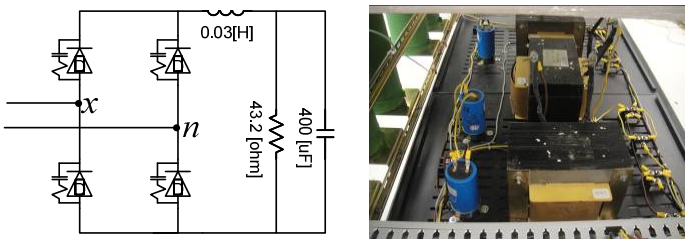
(a) Passive part connection (b) IGBT and its driver

(c) Signal condition board (d) DSP

Figure 8. System construction

From Figure 8 (d), the extension board is used for DSP convenient connection and testing.

The experimental testing load is shown in Figure 9. Figure 10 shows the waveform of the load, TABLE 3 gives the summarization of the load power quality condition. Due to the high frequency harmonic current is too small, therefore the summary of the load power quality condition only includes 3rd, 5th and 7th order harmonic current only.



(a) Single phase connection (b) Three phase connection

Figure 9. Load connection

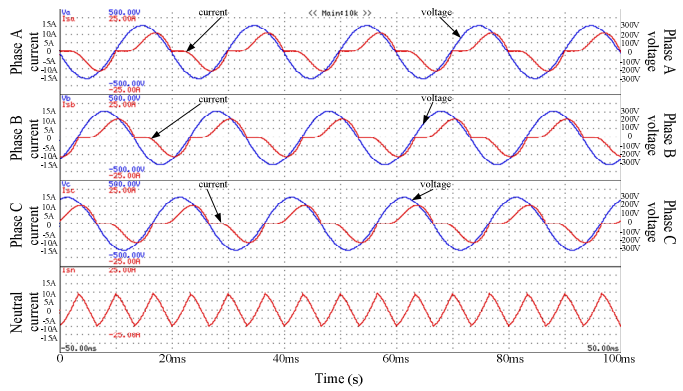


Figure 10. Load waveform

TABLE 3. SUMMARIZAION OF THE LOAD POWER QUALITY CONDITION

Fundamental current	**3rd order harmonic current**	**5th order harmonic current**	**7th order harmonic current**
6.11A	1.92A	0.45A	0.20A
i_{sn} (Neutral current)	**DPF (Power factor)**	**Reactive power**	**THD (Total harmonic distortion)**
5.35A	0.83	830VAR	32.7%

According to (1), (2) and TABLE 3, the design of the coupling capacitor C_c and inductor L_c of the *LC*-HAPF can be expressed as:

$$C_c = \frac{220V^2}{2\pi \cdot 50 \cdot 830VAR} = 5.4uF \approx 50uF$$
$$L_c = \frac{1}{(5 \cdot 2\pi \cdot 50Hz)^2 \cdot 50uF} = 8.1mH \approx 8mH \quad (12)$$

Based on the analysis of the minimum dc-link voltage [13], the minimum dc-link voltage for the *LC*-HAPF to compensate the load is calculated by TABLE 4.

TABLE 4. THE REQUIRED MINIMUM DC-LINK VOLTAGE OF THE *LC*-HAPF

Fundamental reactive current	**3rd order harmonic current**	**5th order harmonic current**	**7th order harmonic current**	**Required V_{dc}**
16.42V	37.15V	0.10V	2.40V	40.77V

After indentified the passive part of the *LC*-HAPF and the reference dc-link voltage, the compensation control algorithm for the *LC*-HAPF will be determined by instantaneous p-q theory [14] and implemented by the DSP, the transient of the load compensation is shown in Figure 11, TABLE 5 gives the summary of the compensation results.

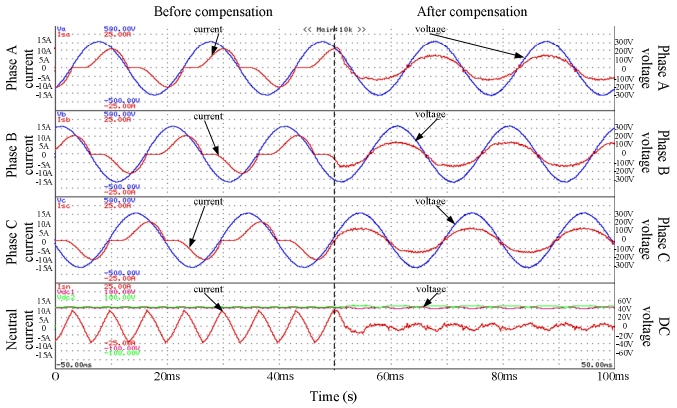


Figure 11. Transient of the load compensation

TABLE 5. SUMMARY OF EXPERIMENT COMPENSATION RESULTS

	V_{dc} (V)	**3rd harmonic (%)**	**5th harmonic (%)**	**DPF**	***THD*$_{isx}$ (%)**	**i_{sn} (Arms)**
Before Comp	---	31.4	7.3	0.83	32.7	5.35
After Comp	45.0	6.3	1.1	1.00	8.0	1.30

According to Figure 11 and TABLE 5, the designed capacitor C_c, inductor L_c and the reference dc-link voltage of the *LC*-HAPF can successfully compensate the loading situation as shown in Figure 9 and 10. Moreover, the compensation results are all satisfied the IEC and IEEE standards [15]-[16].

IV. CONCULATION

This paper introduces the hardware realization of a 10KVA three-phase four-wire center-split *LC*-HAPF. Based on the analysis of the passive part design and the reference dc-link voltage design, according to the load power quality condition, the coupling capacitor C_c, coupling inductor L_c and the reference dc-link voltage V_{dc} can be designed. Under the requirement of the IGBT and the DSP, the IGBT driver and the signal condition board had been introduced. Finally, a three-phase four-wire center-split *LC*-HAPF experiment system has been built. After implementation the compensation control algorithm by the DSP, a good compensation result can be obtained even through the active part of the *LC*-HAPF works on a low dc-link voltage rating.

V. ACKNOWLEDGMENT

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