Stability Study on Dynamic Voltage Restorer (DVR)

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Abstract –This paper discusses the stability study in dynamic voltage restorer (DVR), a series compensation device mainly used to mitigate voltage sags. Based on the appropriate modeling of the DVR system, the detailed stability analysis of the DVR system is performed. This research work is an attempt to obtain mathematical interactions between the DVR and linear loads. In this paper, theoretical study of different linear load effects on the system stability will be proposed and analyzed, in which the stable operation range of the DVR is investigated. Moreover, a significant reduction of inverter gain in the situation of over-modulation can strongly affect the system stability. The results of simulation are presented to validate the load stability analysis and over-modulation effect to the inverter gain, a key parameter affecting the system stability.

Keywords – Dynamic Voltage Restorer (DVR), stability, load, inverter gain, over-modulation, modulation index

NOMENCLATURE

" ^ "	*Peak of the associates waveform*
A_t	*Triangle carrier*
V^*	*Sinusoidal phase voltage command*
M_i	*Modulation index* = $\hat{V}^* / \hat{A}_t$
u_{dc}	*DC bus voltage*
L	*Filtering inductor*
C	*Filtering capacitor*
α	*Filtering capacitor current gain*
β	*Load voltage feedback gain*
K_m	*Fundamental inverter gain*
K_v	*Proportional gain*
K_T	*Voltage transducer gain*
τ	*Time constant in PI controller*

I. INTRODUCTION

A Dynamic voltage restorer (DVR) is a power-electronic-converter-based device, designed to protect critical loads from all supply-side disturbances other than outages. It is connected in series with a distribution feeder and is capable of generating or absorbing real and reactive power at its ac terminals. The basic principle of a DVR is simple: by inserting a voltage of required magnitude and frequency, the DVR can restore the load-side voltage to the desired amplitude and waveform even when the source voltage is unbalanced or distorted. Usually a DVR is connected to protect sensitive loads during faults in the supply system [1].

In the past years, many authors focused on the DVR structure, design schemes, power optimization. And most of them concentrated on the different control methods in order to obtain good system performance [2]-[4], [7]-[9]. In addition, there are very few authors focused on the time delay, damping factor, nonlinear element in the filter inductor [2], [3], which is related to the system stability problem. However, the load impact on the system stability was not included. For the impact of load transients on the DVR, the static load and the induction motor load will exhibit drastic dynamic responses under the voltage phase shift. Greater phase shift changes will produce more drastic oscillations. For parallel loads, the impedance between the source and loads could mitigate the effect of the step voltage phase shift. When the DVR device is installed very close to the loads, the response of loads under the step voltage will cause largest impact on the system [10]. In which this author has considered the effect of load to the system, but not yet set up a generalized stability range for the DVR system.

The objective of this paper is to study and analyze the stability involved in the DVR and to observe the significant effect of the load on the system stability, which may sometimes be neglected. Based on the proposed generalized equation, the theoretical stability study of linear load effect on the system stability via ROUTH-HURWITZ criterion will be presented. The PWM voltage source inverter gain also becomes nonlinear in the over-modulation region, which greatly influences the system stability as well. In addition, the larger the inverter gain K_m, the larger the system stable region will be and obtain better system stability. Finally, the results of simulation are included to show the validity of its stability study.

II. DVR STRUCTURE

Fig. 1 shows the one line diagram of a DVR [5], which consists of a single phase rectifier, single phase inverter, DC storage capacitor, transformer and a pair of filtering capacitor and inductor. And the detail of the DVR circuit configuration can be referred to Reference [5].

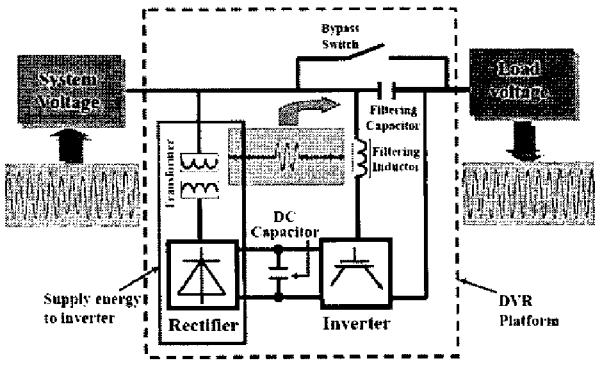

Fig. 1: One line diagram of a Dynamic Voltage Restorer

In addition, the DVR makes use of 3 single-phase inverters to control the voltage insertion to each phase. As each phase operates independently without affecting the other two phases, this benefits in the simplicity and independent control and analysis. Moreover, zero sequence voltage can be injected into the system. Thus, the control analysis of the series inverter configuration can be focused on a single-phase H-bridge inverter [5], [6]. Besides, Fig. 2 demonstrates the equivalent circuit model of a single-phase inverter, while Fig. 3 shows the theoretical diagram of the PWM trigger signal based on regular sampling. With the help of Fig. 2 and Fig. 3, the equivalent model of the inverter can be established.

Define S^* is an ON-OFF function, where

$$S^* = \begin{cases} 1 & S_2S_3 \text{ are closed} \\ -1 & S_1S_4 \text{ are closed} \end{cases} \quad (1)$$

If the peak value of the triangular wave =1, then the sine wave is:

$$U_r = m \sin \omega_r t_d \quad (0 < m < 1) \quad (2)$$

where m and ω_r is the amplitude and angular frequency of the reference voltage, t_d is the average time between two triangle wave peak values.

By using the average of the existing time of two-state values in one switching period to substitute S^*, named it $\overline{S^*}$, then the average $\overline{S^*}$ in one switching period is:

$$\overline{S^*} = m \sin \omega_r t_d \quad (3)$$

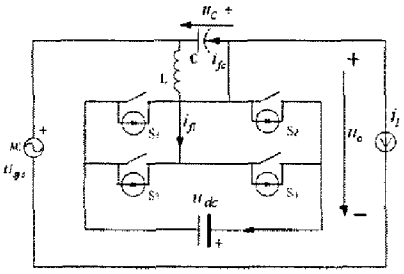

Fig. 2: Equivalent circuit model of a single-phase inverter

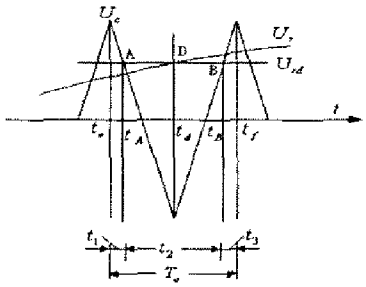

Fig. 3: PWM trigger signal based on regular sampling

From equation (3), the output voltage of the inverter u_{inv} equals $m\sin(\omega_r t_d)u_{dc}$. Thus, the inverter can be equivalent as a gain K_m=u_{dc}, which is linear during analysis. However, in order to have a good load regulation characteristics, fast dynamic response and stable output load voltage, the instantaneous output voltage and the filtering capacitor current i_{fc} are feedback to the system [5], [6]. Finally, Fig. 4 illustrates the DVR system block diagram model.

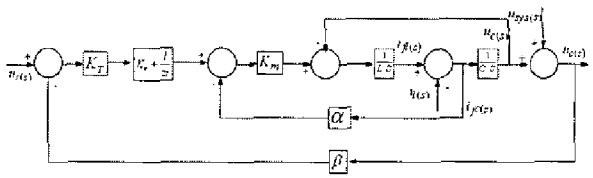

Fig. 4: System block diagram model of the DVR

Based on this system block diagram model, the detail of the system stability will be discussed in the following.

III. Stability Study

In the past, many stability analyses assumed the load current as a constant parameter. However, in reality, load current is not always a constant value. Thus, the load effect to the system stability must be considered. With the system block diagram model shown in Fig. 4, the system stability of the DVR can be analyzed as follows.

A. Conventional Stability Study of DVR

Reference [6] shows the open-loop transfer function G_{or} between u_o and u_r according to Fig. 4:

$$G_{or}(s) = \frac{K_T K_m (1 + K_v \tau s)}{\tau s (LCs^2 + K_m C \alpha s + 1)} \quad (4)$$

With one zero and three poles:

$$S_{oz} = -\frac{1}{K_v \tau} \quad (5)$$

$$S_{op1} = 0,\ S_{op2,3} = -\frac{\alpha K_m}{2L} \pm \sqrt{(\frac{\alpha K_m}{2L})^2 - \frac{1}{LC}} \quad (6)$$

From equation (6), S_{op2} and S_{op3} both have negative real part, which is located in the left s-plane. By changing the parameter, the locations of S_{op2} and S_{op3} will change respectively.

If $(\frac{\alpha K_m}{2L})^2 < \frac{1}{LC}$, that is $2\sqrt{\frac{L}{C}} > \alpha K_m$, the system has a pair of complex poles.

$$S_{op2,3} = -\frac{\alpha K_m}{2L} \pm j\sqrt{-(\frac{\alpha K_m}{2L})^2 + \frac{1}{LC}} \quad (7)$$

If $(\frac{\alpha K_m}{2L})^2 \geq \frac{1}{LC}$, that is $2\sqrt{\frac{L}{C}} \leq \alpha K_m$, the system has two negative real roots.

$$S_{op2,3} = -\frac{\alpha K_m}{2L} \pm \sqrt{(\frac{\alpha K_m}{2L})^2 - \frac{1}{LC}} \quad (8)$$

When the root locus gain approaches to infinite, there are also two root locus approaches infinite as well. Moreover, the slope of two asymptotes (9) is $\pi/2$ and $3\pi/2$ and the intersection point between that two asymptotes and real-axis is σ_a, which can be calculated by equation (10):

$$\varphi_a = \frac{(2k+1)\pi}{n-m} (k = 0,1..., n-m-1) \quad (9)$$

where n = number of finite poles, m= number of finite zeros.

$$\sigma_a = \frac{\sum_{i=1}^{3} S_{opi} - \sum_{j=1}^{1} S_{ozj}}{2} = -\frac{1}{2}\left(\frac{\alpha K_m}{L} - \frac{1}{K_v \tau}\right) \quad (10)$$

Selecting suitable system parameters can guarantee σ_a far away from the jω axis, and maintain a good system stability margin. From the open-loop transfer function (4), the closed-loop transfer function is:

$$G_{cr}(s) = \frac{K_T K_m (1 + K_v \tau s)}{LC\tau s^3 + K_m C\alpha \tau s^2 + \tau s(1 + K_T K_m K_v \beta) + K_T K_m \beta} \quad (11)$$

Table 1. shows a set of designed DVR system parameters, which can be used to analyze the system typically.

Table 1: shows a set of designed system parameters

System Parameters	Values
L	7.6mH
C	11uF
α	26.4
β	1
K_m	25
K_v	15
K_T	0.09565
τ	2ms
Switching frequency f_{sw}	10kHz

Under the system parameters shown in Table 1, the system has two negative real poles, and the two asymptotes intersect at a common point on the real axis of σ_a = -4.34 × 10^4 rad/s, which guarantees the root locus far away from the jω axis in the s-plane.

According to the closed-loop transfer function (11), Fig. 5 demonstrates the root locus diagram of the system under the designed parameters mentioned in Table 1. From Fig. 5, the zero and the three poles S_{cz}, S_{cp1}, S_{cp2}, S_{cp3} values are -33.3 rad/s, -32.6 rad/s, -5.38 × 10^3 rad/s and -8.14 × 10^4 rad/s, which the poles S_{cp2}, S_{cp3} are far away from the jω axis. Using σ_a to express the intersection point between the asymptotic and real-axis, which is located between the two poles S_{cp2}, S_{cp3}. Therefore, if the open-loop gain changes, the closed-loop poles will change according to $S_{cp3} \rightarrow \sigma_a \rightarrow +\infty$ and $S_{cp2} \rightarrow \sigma_a \rightarrow -\infty$ respectively, but the position of the pole S_{cp1} does not vary a lot. As a result, poles S_{cp2}, S_{cp3} can be said as the dominated poles.

Fig. 5 and Fig. 6 show the bode diagrams of the open-loop and closed-loop system. From open-loop bode plot, the system is stable due to having a rather large stability margin of Gm=inf dB, Pm=88.0°. And from the closed-loop bode plot, the system output voltage can track the reference voltage and have a good low-pass characteristic at the low frequency band.

According to the block diagram model in Fig. 4, if the load current i_l is assumed to be a constant parameter and the DVR system is designed according to those parameters in Table 1, the DVR system will always be stable.

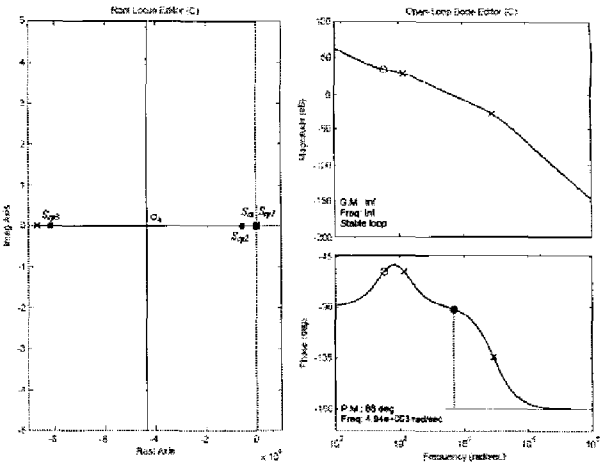

Fig. 5: Root locus diagram of the system

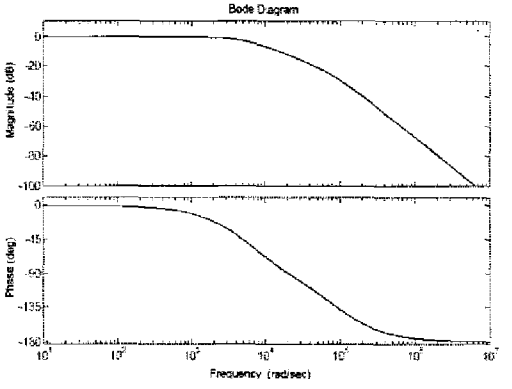

Fig.6: Bode diagram of the closed-loop system

B. Unstable Phenomenon of the DVR

However, i_l is not always a constant value in reality. Therefore, an unconventional stability study will be introduced in this part. When load is also considered inside the system, the system block diagram model shown in Fig. 4 can be modified into the one shown in Fig. 7.

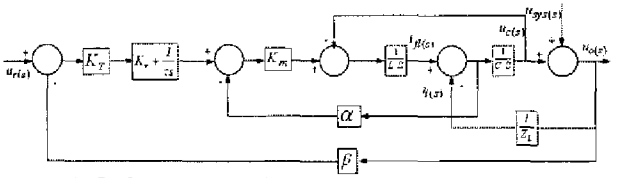

Fig.7: System block diagram with including the load

Considering the general steady state case of the system block diagram including the load, $Z_L = R + 1/X$. When the load consists of inductive element, $X = (sL_L)^{-1}$ and $Z_L = R + 1/(sL_L)^{-1}$. When the load consists of capacitive element, $X = sC_L$ and $Z_L = R + 1/sC_L$. Then the general open-loop and closed-loop transfer function G_{or} and G_{cr} between u_o and u_r is:

$$G_{or}(s) = \frac{K_T K_m (1 + K_v \tau s)(1 + RX)}{\tau s\left((1 + RX)CLs^2 + (CK_m \alpha (1 + RX) + LX)s + (1 + RX)\right)} \quad (12)$$

$$G_{cr}(s) = \frac{K_T K_m (1 + K_v \tau s)(1 + RX)}{(1 + RX)LC\tau s^3 + (LX + \alpha CK_m (1 + RX))\tau s^2 + ((\beta K_m K_v K_T + 1)(1 + RX))\tau s + \beta K_m K_T (1 + RX)} \quad (13)$$

When the system has no load condition that is R = 0 and X= 0, the open-loop and closed-loop transfer function is:

$$G_{or}(s)=\frac{K_T K_m(1+K_v\tau s)}{\tau s\left(LCs^2+K_m C\alpha s+1\right)} \tag{14}$$

$$G_{cr}(s)=\frac{K_T K_m(1+K_v\tau s)}{LC\tau s^3+K_m\alpha C\tau s^2+(\beta K_m K_v K_T+1)\tau s+\beta K_m K_T} \tag{15}$$

which are consistent with (4) and (11). As a result, the system stability study with linear load R, L, C can be based on the general transfer functions (12) and (13).

According Fig. 7, and the system parameters mentioned in Table 1, the system stability with each type of linear load has been analyzed. In which, the R, L load will not lead to an unstable system. Unfortunately, pure capacitive load will yield a stability problem to the system. Thus the following stability analysis will only be focused on the pure capacitive load situation.

For pure capacitive load C_L, the closed-loop transfer function is:

$$G_{cr}(s)=\frac{K_T K_m(1+K_v\tau s)}{(C+C_L)L\tau s^3+\alpha CK_m\tau s^2+(\tau+\beta K_m K_T K_v\tau)s+\beta K_m K_T} \tag{16}$$

By ROUTH-HURWITZ criterion, the Routh table can be obtained as follows:

s^3	$(C+C_L)L\tau$	$\tau+\beta K_m K_T K_v\tau$
s^2	$\alpha CK_m\tau$	$\beta K_m K_T$
s^1	$\frac{\alpha Ck_m\tau^2(1+\beta K_m K_T K_v)}{\alpha CK_m\tau}$	
	$-\frac{(C+C_L)L\tau\beta K_m K_T}{\alpha CK_m\tau}$	
s^0	$\beta K_m K_T$	

The closed loop system is stable if and only if there are no sign changes in the first column of the above table. Thus, the system must fulfill the following four conditions:

Condition 1: $(C+C_L)L\tau>0$

Condition 2: $\alpha CK_m\tau>0$

Condition 3:

$$\frac{\alpha Ck_m\tau^2(1+\beta K_m K_T K_v)-(C+C_L)L\tau\beta K_m K_T}{\alpha CK_m\tau}>0$$

Condition 4: $\beta K_m K_T>0$

According to the system parameters illustrated in Table 1, Conditions 2 and 4 are satisfied. And the range of the pure capacitive load can be found by Condition 1 and Condition 3, which is $0<C_L<29.5$mF. Inside this range, the system is stable.

When C_L = 29.4mF, the zero and the three poles S_{cz}, S_{cp1}, S_{cp2}, S_{cp3} values are -33.3 rad/s , -32.4 rad/s, -0.0251+406i rad/s and -0.0251-406i rad/s, in which the two dominated poles locate close to the jω axis with small stability margin of Gm=0.523dB, Pm=0.0073°, shown in Fig. 8a and Fig. 8b. Thus the system is marginally stable because it just falls inside the range $0< C_L <29.5$mF.

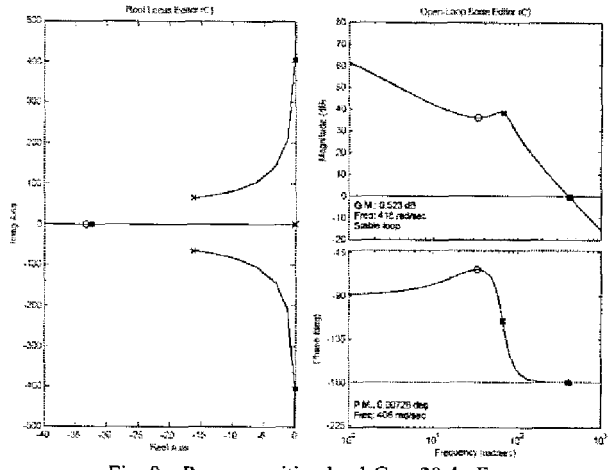

Fig. 8a: Pure capacitive load C_L = 29.4mF

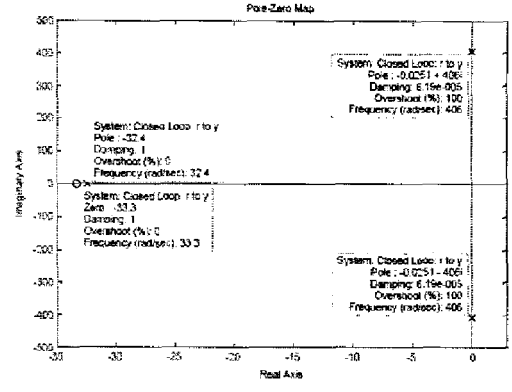

Fig. 8b: Pole-Zero map of pure capacitive load C_L = 29.4mF

By ROUTH-HURWITZ criterion, the stable DVR operation range for pure capacitive load can be found, which is between $0<C_L<29.5$mF. Even though the analysis results in part A show the system very stable, it will become unstable when capacitive load value of $C_L>29.5$mF is connected to the system. Therefore, it is significant to apply both the conventional and proposed method in the whole system stability study.

C. Stable and Unstable Regions

According to Fig. 3, the sine wave modulated PWM inverter may be represented by the following set of equations: first a describing function [11]

$$G(M_i)=\frac{2}{\pi}\left\{\sin^{-1}\left(\frac{1}{M_i}\right)+\frac{1}{M_i}\sqrt{1-\frac{1}{M_i^2}}\right\} \tag{17}$$

When the sinusoidal phase voltage command $V^*<\hat{A}_t$, peak of triangle carrier, under-modulation occurs with the modulation index $M_i \le 1$, then the fundamental inverter gain K_m is linear, which gives equation (18)

$$G_{nom}(u_{dc})=\frac{u_{dc}}{\hat{A}_t}=K_m \tag{18}$$

However, when the sinusoidal phase voltage command $V^*>\hat{A}_t$, over-modulation occurs with the modulation index $M_i>1$, then the fundamental inverter gain K_m is nonlinear, which gives equation (19)

$$G(u_{dc},M_i)=G_{nom}(u_{dc})\times G(M_i)=K_m \tag{19}$$

In section II, the inverter is equivalent as a linear gain, which simplifies the inverter model for analysis. In order to guarantee the theoretical capacitive load range $0<C_L<29.5$mF workable in the designed DVR system, the fundamental inverter gain must be linear (18). Fig. 9 clarifies the general stable and unstable regions study for capacitive load values with different inverter gain.

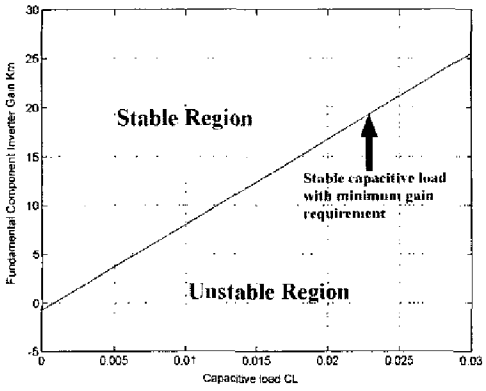

Fig. 9: General stable and unstable regions for inverter gain K_m vs capacitive load C_L

Based on the nonlinear inverter gain equation (19), Fig. 10 shows that the fundamental inverter gain K_m varies with the modulation index M_i.

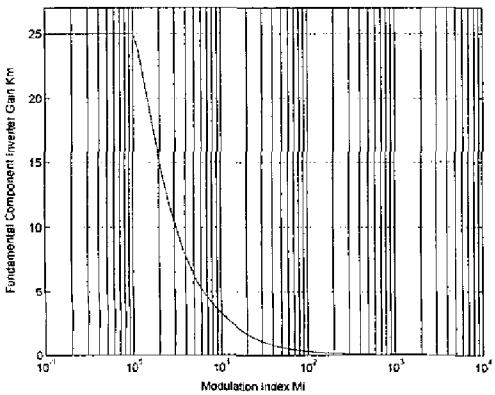

Fig. 10: Fundamental inverter gain K_m varies with the modulation index M_i

From Fig. 10, when the modulation index appears to be $M_i \leq 1$ (under-modulation), the inverter gain is linear and keeps at a constant value. Then the support stable capacitive load range will be $0<C_L<29.5$mF illustrated by Fig. 9, which matches with the theoretical results in section III. But when the modulation index continues to increase from unity (over-modulation), the inverter gain will decrease exponentially, shown in Fig. 10. This results in a great reduction of stable capacitive load range, which can also be illustrated clearly in Fig. 9.

In addition, when over-modulation occurs, the inverter gain becomes nonlinear. Then the system block diagram model of Fig. 4 and Fig. 7 cannot be used to describe the practical DVR system anymore. Moreover, they are no more suitable for the system stability analysis. For the design of the DVR, the effect of the inverter gain in both under-modulation and over-modulation to the system stability should be considered carefully.

IV. Simulation Results And Discussion

When over-modulation occurs in the state of $M_i > 1$, the inverter gain becomes nonlinear. As a result, the DVR system has the possibility to be unstable even inside the theoretical stable range $0<C_L<29.5$mF. This unstable phenomenon may cause large amount money lost due to the abnormal operation of very sensitive loads and high precision productive machines. In more serious situation, it may burn the sensitive loads which are originally protected by the DVR. As a result, it is essential and important to study the stability relationship between over-modulation and inverter gain besides the load effect.

As the capacitive load value keeps at a constant value of 20mF, the fundamental inverter gain changes to 5, 17.5 and 25 respectively. Fig. 11a, Fig. 11b and Fig. 11c illustrates the simulation results of three different cases.

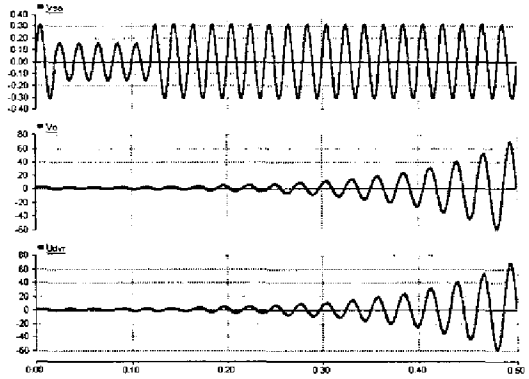

Fig. 11a: Unstable output voltage at C_L=20mF, K_m = 5

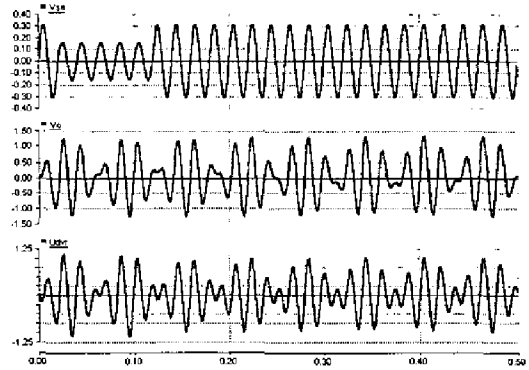

Fig. 11b: Marginally Stable output voltage at C_L=20mF, K_m = 17.5

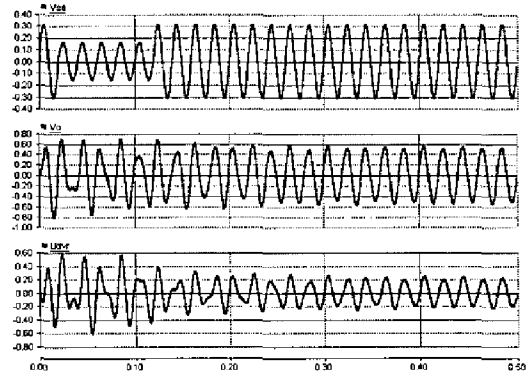

Fig. 11c: Stable output voltage at C_L=20mF, K_m = 25

When the inverter gain K_m =5, the system is unstable as the output load voltage oscillates to a simultaneously larger magnitude, shown in Fig. 11a. However, when the inverter gain K_m increases to 17.5, the system is marginally stable because the output load voltage oscillates without getting to a larger value, shown in Fig. 11b. Finally, when the inverter gain K_m increases to 25, the system is stable as the output load voltage reaches to a steady state after 0.3s, which is shown in Fig. 11c. During the first 0.2s, the output load voltage seems to be oscillating, but actually it is just the transient of the system. As the inverter gain K_m is getting larger, the output load voltage will be more stable and vice versa. This reflects the effect of inverter gain K_m to the system stability, and is also consistent with Fig. 9. As the inverter gain goes larger, more capacitive load values will fall inside the stable region.

This research paper indicates that the inverter gain K_m is the key parameter to determine the system stability. The larger the inverter gain, the larger the stable region will be. If the gain decreases to a low value, the system will be easily unstable. In practical case, increasing the bus voltage can increase the inverter gain, which provides a larger stability margin to the system. However, increasing the bus voltage added to the cost of the control to maintain a higher bus voltage, a cost and size penalty are also paid for the dc bus capacitor banks, along with increased switching losses [12], which are the disadvantages.

For the design of the DVR, many researchers only study the stability of the DVR system itself, without considering about the load effect to the whole system. Even though the DVR has a very stable situation during no load condition, it may still contain stability problem when the load is connected. Thus, this paper also aims to illustrate this idea.

Inside this designed stable DVR system, the stable operation range for the resistive or inductive load value are $R>0$ and $L_L>0$. Although the stable range for pure capacitive load is between $0<C_L<29.5$mF, the phenomenon of over-modulation will greatly reduce the stable capacitive range by a significant reduction in inverter gain.

V. Conclusion

Based on the block diagram model and proposed generalized equation of the DVR, the theoretical study of the linear load on the system stability is investigated. Moreover, the effect of inverter gain to the system stability in both regions is also presented. In order to have a very stable system, the inverter gain should be as large as possible. Finally, the simulation results agree with the theoretical prediction and verify all the stability analysis.

This paper only discusses the stability range in linear load situation and the effect of over-modulation to the system. Future work will focus on finding a method to extend the linearity during over-modulation, and the nonlinear load, load transients effect to the DVR stability.

VI. Acknowledgment

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VII. References

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