Theoretical Study of
3 Dimensional Hysteresis PWM Techniques

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Abstract — **In this paper, the theoretical study and comparison between the a-b-c Hysteresis PWM technique which is proposed in [1] at 1997 and 3 Dimensional (α-β-0) Hysteresis PWM which is proposed in [2] at 1998 are performed for 3-Phase 4-Wire 3-Leg Center-Split Power Quality Compensators. There is description on dc voltage variation control in the a-b-c Hysteresis PWM technique, however, no description of dc voltage variation and no determination of error bands are performed for 3-Dimensional (α-β-0) Hysteresis one. In this paper, a novel 3D Hysteresis Control is proposed with dc voltage control by the concept of keeping the same overall error bounded volume with higher the dc control ability.**

Keywords - PWM; 3-Phase 4Wire System; Power Quality Compensator ;dc Voltage Variation;

I. INTRODUCTION

In past researches, almost all the studies of PWM control strategies are focused on 3-phase 3-wire systems. However, there are 3-phase 3-wire and 3-phase 4-wire systems in electric power networks. Normally the shunt connected power quality compensator is to improve the current quality. In 3-phase 3-wire system, the current quality issues are reactive, unbalance and harmonic currents. However, the neutral current compensationshould be included in the 3-phase 4-wire system as well as the above described current issues. In 1997, 4-Leg and 3-Leg Center-Split Inverters are proposed to compensate the reactive, unbalance, harmonic and neutral currents in 3-phase 4-wire systems [1]. In [1], there is a-b-c Hysteresis Control Method to improve the current quality as well as to control the d. c. voltage variation by a 3-Leg Center-Split Inverter. Afterwards, in 1998, the α-β-0 Hysteresis Control strategy is proposed for controlling the 3-Leg Center-Split Inverter [2]. Although this α-β-0 Hysteresis Control strategy [2] can improve the current issues, there is no description on a α-β-0 controlled method for reducing the d. c. voltage variation of the 3-Leg Center-Split Inverter. In this paper, the novel α-β-0 Hysteresis method for controlling the d. c. voltage variation as well as the current quality compensation of 3-Leg Center-Split Inverter is proposed, and the comparison between the a-b-c and α-β-0 Hysteresis Control Methods is performed. The theoretical studies for compensation performance and reasonable settlement of Hysteresis-Error-Bands are achieved.

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II. COMPARISON BETWEEN 4-LEG AND 3-LEG CENTER-SPLIT INVERTERS

In this section, the comparison between 4-Leg and 3-Leg Center-Split Inverters is performed in respect to their 2-level and 3-level Neutral-Point-Clamped (NPC) structures.

A. 2-Level System

Fig. 1 and Fig. 2 show the circuit configurations of 2-level 4-Leg and 3-Leg Center-Split Inverters respectively.

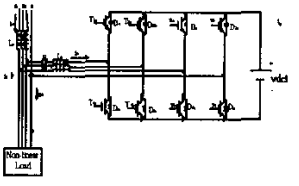

Fig. 1 2-Level 3-Phase 4-Wire 4-Leg Inverter

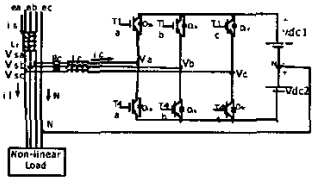

Fig. 2 2-Level 3-Phase 4-Wire 3-Leg Center-Split Inverter

Regarding to their structures, one leg of a 4-leg inverter is dedicated to compensate the neutral current so as to increase the initial cost of inverters for switching components. However, in 3-Leg Center-Split Inverter, a large neutral current due to serious unbalance loads affects the d. c. voltage variation so that larger capacitors are needed to maintain the d. c. voltage variation within an acceptable level. Comparatively, the initial cost of dedicating one more leg of switching components in 4-Leg system may be higher than the cost of increasing the capacitance in 3-Leg Center-Split one. With regard to changing the switching states of 3-Leg Center-Split Inverter, the current that includes the harmonic, unbalance, reactive and neutral current components, and d. c. voltage is affected simultaneously. The control algorithm of 3-Leg

Center-Split one will be more complicated than a 4-Leg case. Furthermore, there is less d. c. voltage utilization ratio in 3-Leg. As a result, more research approaches have been taken for the 4-Leg system [3].

B. 3-Level NPC System

Basically, the above discussion and conclusion are performed under the 2-level circuit configuration. Moreover, if 3-Level NPC inverter is taken into consideration, the outcomes may be different. Fig. 3 shows the circuit configuration of a Tri-level NPC Power Quality Compensator by a 3-Leg Center-Split structure.

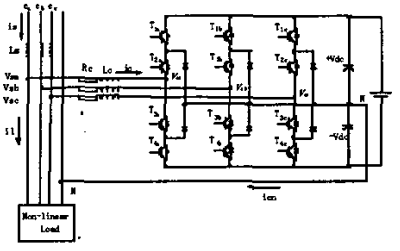

Fig. 3 3-Phase 4-Wire 3-Level NPC 3-Leg Center-Split Inverter

The benefits by using a Tri-level NPC 3-Leg Center-Split Inverter are:

1) A Tri-level NPC structure inverter can be operated in a 3-Phase 3-Wire or 3-Phase 4-Wire mode. Connecting a wire between the mid-point of d. c. capacitors and the neutral line, it turns into a 3-Phase 4-Wire system. Without that neutral wire, it will be a 3-Phase 3-Wire system.

2) Fewer switching components are needed in comparison with a 4-Leg Tri-Level NPC structure.

3) There is the same d. c. voltage utilization for 3-Phase 3-Wire and 3-Phase 4-Wire Tri-level systems.

4) It has higher voltage capacity, higher waveform quality and lower switching losses than a 2-level one.

Nevertheless, the control algorithm will be more complicated.

III. HYSTERESIS PWM TECHNIQUES

A. a-b-c Hysteresis Control

According to the past research [4], the instantaneous compensation in a-b-c coordinates can be performed by Generalized Instantaneous Reactive Power Theory that is proposed for instantaneous detection of injected current components from the shunt inverter. However after the detection of instantaneous a-b-c coordinated currents for compensation is performed, the switching components of a Tri-level NPC 3-Leg Center-Split Inverter should be controlled by an appropriated PWM technique to generate the compensated current into the practical system to improve the current quality. One of the effective and simple ways is the Hysteresis PWM Control. There are a-b-c and α-β-0 Hysteresis PWM strategies.

In a-b-c coordinates, the upper and lower error bands or tolerances of Hysteresis methods can be defined as following.

$$\text{Upper Band Limit}: \quad i_{ck} + B/2 \tag{1}$$

$$\text{Lower Band Limit} \quad i_{ck} - B/2 \tag{2}$$

, where i_{ck} (k=a,b,c) is the compensated reference and B is the total error-allowable band width.

Transforming the a-b-c error bands into α-β-0 for comparison is achieved according to (1), (2) and (3).

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{3}$$

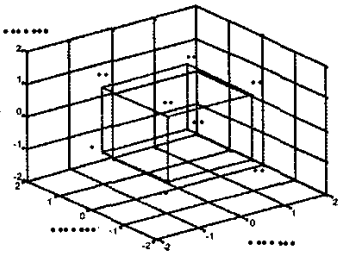

Fig.4 Error Volume in a-b-c coordinates

The 3 dimensional a-b-c Hysteresis Error Volume can be transformed into α-β-0 coordinate as shown in Fig. 4.

B. α-β-0 Hysteresis Control

In α-β-0 Hysteresis Control, the error bands, (4) and (5), are defined in α-β-0 coordinates, not a-b-c coordinates.

$$\text{Upper Band Limit}: \quad i_{cm} + B/2 \tag{4}$$

$$\text{Lower Band Limit} \quad i_{cm} - B/2 \tag{5}$$

, where i_{cm} (m=α,β,0) is the compensated reference and B is the total error-allowable band width.

The 3 dimensional α-β-0 Hysteresis Error Volume can be defined in α-β-0 coordinates as shown in Fig. 5. In Fig. 4, Fig. 5 and all the following figures, B is defined as 2 units accordingly.

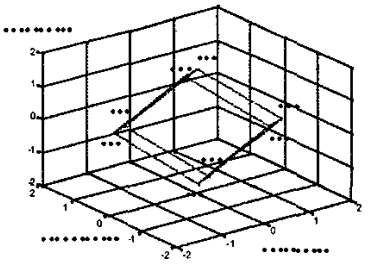

Fig.5 Error Volume in α-β-0 coordinates

C. *Error Comparsion between a-b-c and α-β-0 Hysteresis Techniques*

Table 1 shows error locations transferred from a-b-c into α-β-0 coordinates. Fig. 6.a, Fig. 6.b, Fig. 6.c and Fig. 6.d. show the left, right, top views and a 3-dimensional vision of the error band 3-D figures respectively.

Table 1 a-b-c and α-β-0 Error Location in α-β-0 coordinate

Location in Fig. 6	a	b	c	Location in Fig. 6	α	β	
a	$+B/2$	$+B/2$	$+B/2$	a1	0	0	$\sqrt{3}\frac{B}{2}$
c	$+B/2$	$+B/2$	$-B/2$	c1	$\sqrt{\frac{2}{3}}\frac{B}{2}$	$\frac{B}{\sqrt{2}}$	$\frac{1}{\sqrt{3}}\frac{B}{2}$
g	$+B/2$	$-B/2$	$+B/2$	g1	$\sqrt{\frac{2}{3}}\frac{B}{2}$	$-\frac{B}{\sqrt{2}}$	$\frac{1}{\sqrt{3}}\frac{B}{2}$
h	$+B/2$	$-B/2$	$-B/2$	h1	$\sqrt{\frac{2}{3}}B$	0	$-\frac{1}{\sqrt{3}}\frac{B}{2}$
b	$-B/2$	$+B/2$	$+B/2$	b1	$-\sqrt{\frac{2}{3}}B$	0	$\frac{1}{\sqrt{3}}\frac{B}{2}$
d	$-B/2$	$+B/2$	$-B/2$	d1	$-\sqrt{\frac{2}{3}}\frac{B}{2}$	$\frac{B}{\sqrt{2}}$	$\frac{1}{\sqrt{3}}\frac{B}{2}$
e	$-B/2$	$-B/2$	$+B/2$	e1	$-\sqrt{\frac{2}{3}}\frac{B}{2}$	$-\frac{B}{\sqrt{2}}$	$\frac{1}{\sqrt{3}}\frac{B}{2}$
f	$-B/2$	$-B/2$	$-B/2$	f1	0	0	$-\sqrt{3}\frac{B}{2}$

The compensation performance of those two Hysteresis PWM methods can be compared in accordance with their 3 dimensional error volumes shown in Fig. 6.

In the consideration of calculating the error volume, B^3 is the total error volume for α-β-0 Hysteresis Control Method as the error shape is cubical. On the other hand, the error volume of a-b-c Hysteresis method can be computed by considerations of the Linear Transformation and the computation of the Norm of Jacobian Matrix. Equation (6) is for getting the error volume.

$$V_{ABC} = \iiint_V f(a,b,c)\,da\,db\,dc \qquad (6)$$

The linear transformation is taken from a-b-c into α-β-0 coordinates. Furthermore, the norm of Jacobian Matrix is needed to compute the error volume.

$$V_{abc} = \iiint_V f(a,b,c)\frac{D(a,b,c)}{D(\alpha,\beta,0)}\,d\alpha\,d\beta\,d0 \qquad (7)$$

, where

$$\frac{D(a,b,c)}{D(\alpha,\beta,0)} = \left(\frac{D(\alpha,\beta,0)}{D(a,b,c)}\right)^{-1} = \begin{vmatrix} \frac{\partial\alpha}{\partial a} & \frac{\partial\alpha}{\partial b} & \frac{\partial\alpha}{\partial c} \\ \frac{\partial\beta}{\partial a} & \frac{\partial\beta}{\partial b} & \frac{\partial\beta}{\partial c} \\ \frac{\partial 0}{\partial a} & \frac{\partial 0}{\partial b} & \frac{\partial 0}{\partial c} \end{vmatrix}^{-1}$$

According to the computation of the Norm of the Jacobian Matrix, the Norm is equal to 1 so that

$$V_{abc} = V_{\alpha\beta 0} = B^3 \qquad (8).$$

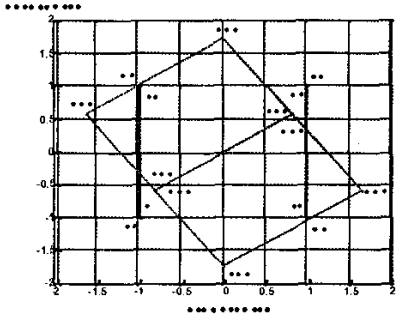

Fig. 6.a Left View

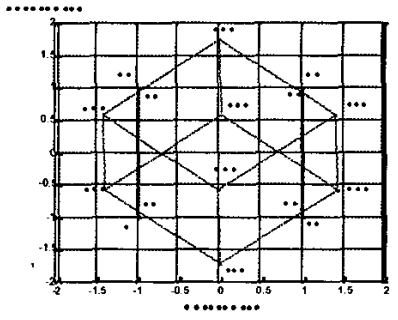

Fig. 6.b Right View

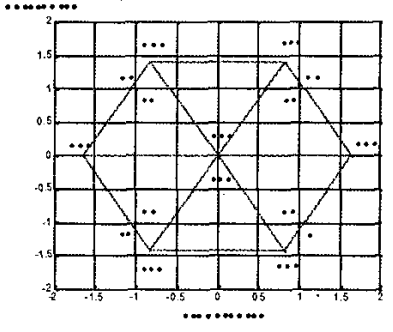

Fig. 6.c Top View

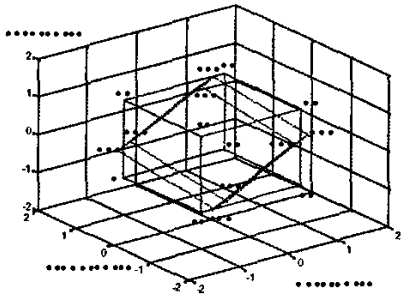

Fig. 6.d 3D Vision

Fig. 6 a-b-c and α-β-0 Error Volumes in α-β-0 coordinate

Furthermore, the comparison between horizontal cross-sectional areas of error volumes of those two a-b-c and α-β-0 Hysteresis methods can be performed as follows. The horizontal cross-sectional area of a-b-c Error Volume within the region shown in Fig. 7 is larger than the cross-sectional area of α-β-0 one that is B^2. However, outside of that region, the horizontal cross-sectional area of the α-β-0 is larger than that of the a-b-c one.

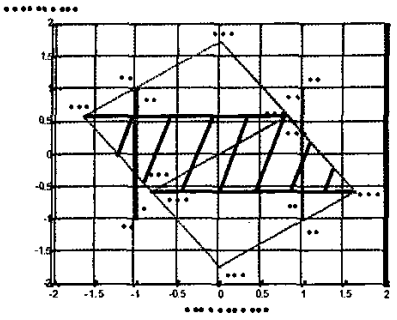

Fig. 7 Horizontal Sectional Area Consideration

According to the above discussion regarding to their maximum error amplitudes, horizontal cross-sectional areas and total error-volumes, the following conclusions of Hysteresis PWM methods can be summarized as:

1) Both Hysteresis PWM methods have the same overall compensated performance regarding to the compensation of harmonic and neutral currents under the consideration having the same error volume, B^3.

2) In a 3-Phase 3-Wire system or a 3-Phase 4-Wire system that has no or small neutral current, α-β or α-β-0 Hysteresis PWM method will have better harmonic compensated performance than the a-b-c one as the α-β-0 has lower horizontal cross-sectional area.

3) In a 3-Phase 4-Wire system that has larger neutral current, the neutral current compensation ability of the α-β-0 Hysteresis method is higher. By the α-β-0 Hysteresis method, the compensated neutral current can be smaller as boundaries of α-β-0 one are smaller along the zero axis. But, α-β-0 one has lower harmonic compensated performance.

IV. D. C. LINKED VOLTAGE CONTROL

A. Conventional a-b-c Hysteresis Control

Based on a three-leg center-split inverter, the current of each phase flows either through C_1 or C_2 and returns through the ac neutral wire, which causes dc voltage variations. Fig. 8 shows the current passing through the upper or lower capacitor so as to cause the dc voltage variation. When i_{ik} 0, v_{c1} rises and v_{c2} decreases, but not with equal ratio due to different phase voltages. The dc voltage variation depends on the shape of the current reference and the Hysteresis bandwidth.

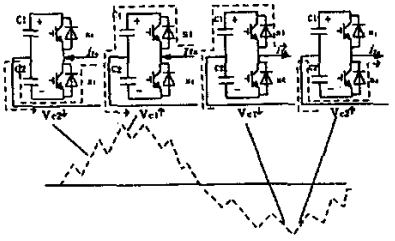

Fig. 8 Hysteresis-band PWM current in one phase

$i_{fk} > 0$ and $\frac{di_{fk}}{dt} < 0$	increase the voltage in C_1
$i_{fk} < 0$ and $\frac{di_{fk}}{dt} < 0$	decrease the voltage in C_1
$i_{fk} < 0$ and $\frac{di_{fk}}{dt} > 0$	increase the voltage in C_2
$i_{fk} > 0$ and $\frac{di_{fk}}{dt} > 0$	decrease the voltage in C_2

Table 2 Variation Conditions for Capacitor Voltages

The conventional control strategy is to define a signal ε that actuates a dynamic offset level. The i_{ck} is the reference current, k can be phase "a", "b" or "c" and B is the Hysteresis Band. The (9) and (10) are the upper band and lower band limits respectively.

$$i_{ck} + \frac{B}{2}(1+\varepsilon) \qquad (9)$$

$$i_{ck} - \frac{B}{2}(1-\varepsilon) \qquad (10)$$

When $\varepsilon > 0$, v_{c1} increases and v_{c2} decreases, and vice versa.

B. α-β-0 Hysteresis Control

In this section, the width of B is defined as the same as the pervious one for comparison (11). The dc voltage variation affects zero sequence only, which was found in [5] so that the proposed strategy in this paper is to alter zero sequence band limit only according to the dc voltage variation, as shown in (12), (13) and (14), so that the Hysteresis Error Volume, Fig. 9, can be shifted upwards or downwards accordingly. When Hysteresis Error Volume is shifting downwards as shown in Fig. 10, the upper-arm capacitor has more changes to be selected to discharge so that the upper-capacitor voltage is decreasing and vice versa.

$$B = 2 \quad \alpha = 2 \quad \beta = 2\Delta 0 \qquad (11)$$

$$a = \quad = B/2 \qquad (12)$$

$$0_{\text{upper-band}} = \frac{B}{2}(1+e) \qquad (13)$$

$$0_{\text{lower-band}} = -\frac{B}{2}(1-e) \qquad (14)$$

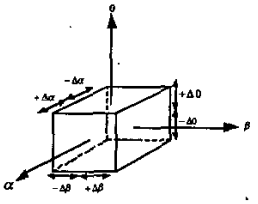

Fig. 9 3D Hysteresis Error-Band

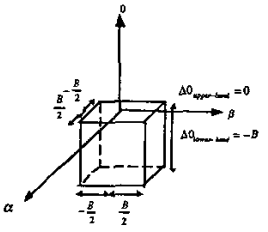

Fig. 10 3D Hysteresis Error Band Shifting Downward

The voltage variation is defined as (15). Table 3 summarized the conditions for controlling dc voltage variation, where V_{ref} is the dc bus voltage reference, V_{max} is the maximum limit of ΔV, and k is between 0 and 1.

$$V = |v_{dc1}| - |v_{dc2}| \qquad (15)$$

V. COMPARISON AND PROPOSED METHOD

The comparison is performed on αβ0 coordinates, which means that the abc Hysteresis band width limits are transferred into αβ0 one.

Hysteresis Controls	Max(α) Error	Max(β) Error	Max(0) Error	$Vol_{\alpha\beta 0}$	D.C. Control
abc	$\sqrt{\frac{2}{3}}B$	$\frac{1}{\sqrt{2}}B$	$\sqrt{3}B$	B^3	$\sqrt{3}\varepsilon$
αβ0	B	B	B	B^3	ε

Table 4 Error-Band Comparisons

It found that maximum error band widths of α and β axes are lower bythe abc Hysteresis method but with higher zero error band width than the αβ0 Hysteresis Method. When it needs to control higher dc voltage variation, all error band widths must be altered by the abc Hysteresis method. As a result, the harmonic and neutral currents are increased so as to degrade the compensation performance. However, the dc voltage control ability is higher by abc Hysteresis method with the same error band volume. In the view point of compensation performance and same error-band volume, the overall performance can be near to each other, but abc Hysteresis method gives better performance in reducing THD contents of currents. However, neutral current is higher. Table 5 summarized the results.

Hysteresis Controls	THD	Neutral Current	Total Error	DC voltage Control Ability
abc	Lower	Higher	Same	Higher
αβ0	Higher	Lower	Same	Lower

Table 5 Performance Comparisons

Furthermore, αβ0 Hysteresis method can be more flexible than abc one as only the error-band along the zero axis can be changed according to the dc voltage variation. The proposed strategy is to tighten the error-bands in α and β axes with $\sqrt{2/3}B$ and $1/\sqrt{2}B$ respectively, then to widen the zero error-band with $\sqrt{3}B$. As a result, αβ0 Hysteresis method has the same error volume with the abc one so that it has the same overall compensated performance, but with higher dc voltage control ability.

VI. SIMULATION AND E PERIMENTAL RESULTS

Simulations are performed by Matlab. Fig. 11 shows the current waveforms before compensation. Fig. 12 and Fig. 13 show the current waveforms after compensation by abc and αβ0 Hysteresis Techniques respectively. The α-β-0 Hysteresis PWM method will have better neutral current compensated performance than the a-b-c, but a-b-c one has better harmonic compensated performance as the α-β-0 has a lower horizontal cross-sectional area. Table 6 summarized the results. They got almost the same overall performance, but a-b-c one has the lower THD and higher neutral current.

The results demonstrate the validity of the above discussions. Fig. 14 shows the dc voltage variation control by the αβ0 Hysteresis Technique. It shows that the proposed technique can control the dc voltage variation. Fig. 15 and Fig. 16 give the experimental results by the proposed αβ0 Hysteresis Control Technique with the dc voltage control algorithm

Cases		Largest Lower Voltage Imbalance	Larger Lower Voltage Imbalance	Larger Upper Voltage Imbalance	Largest Upper Voltage Imbalance
Condition		$-V_{max} < V < -kV_{ref}$	$-kV_{ref} < V < 0$	$0 < V < kV_{ref}$	$kV_{ref} < V < V_{max}$
e		1	$-\frac{V}{kV_{ref}}$	$-\frac{V}{kV_{ref}}$	-1

Table 3 αβ0 DC voltage control strategy

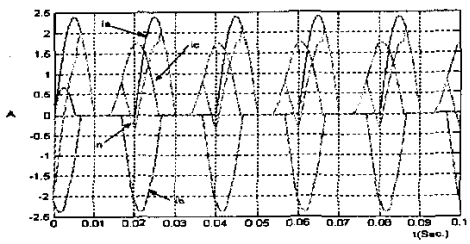

Fig. 12 Current Waveforms before Compensation

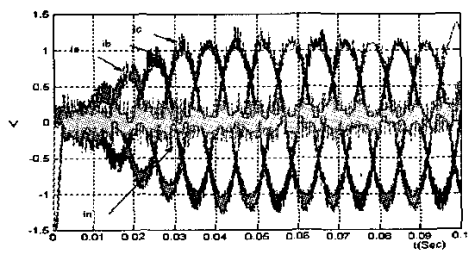

Fig. 12 Compensation by abc Hysteresis Technique

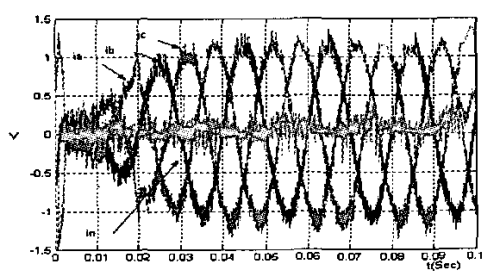

Fig. 13 Compensation by αβ0 Hysteresis Technique

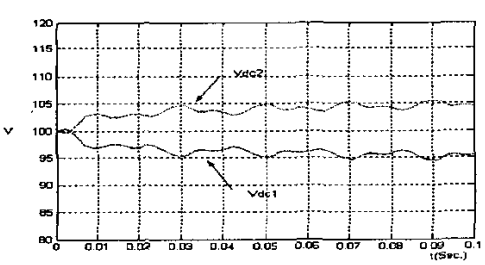

Fig. 14 DC Voltage Variation Control

	Before Compensation	a-b-c Hysteresis control	α–β–0 Hysteresis control
THDa ( )	49.81	9.46	12.72
THDb ( )	50	9.63	9.31
THDc ( )	51.35	12.14	11.53
Absolute Average Zero Error	0.662	0.123	0.0853
Absolute Average Total Error	2.305	0.326	0.315

Table 6 Summarization of Simulated Results

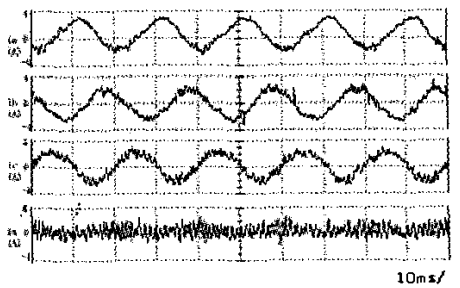

Fig. 15 Experimental Results for Compenastions

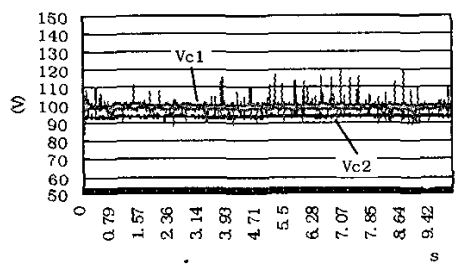

Fig. 16 Experimental Result to control dc Voltage Variation

VII. CONCULSION

The main conclusions can be given as follows:

1) In a-b-c Hysteresis Control Technique, the performance of neutral compensation is not so good as the α–β–0 technique,
2) The α–β–0 Hysteresis method gives higher THD values after compensation.
3) The ability of D.C. voltage variation control by a-b-c Hysteresis Control Technique is higher than the original cubical α–β–0 one,

However, by overcoming the above drawback of the α–β–0 control technique, a novel Rectangular Hysteresis Band Volume is proposed instead of the original cubical 3-D technique.

REFERENCES

[1] Mauricio Aredes, Jurgen Hafner, Klemens Heumann, "Three-Phase Four-Wire Shunt Active Filter Control Strategies," IEEE Trans. on Power Electronics, Vol. 12, No. 2, March 1997, pp. 311-318.

[2] P. Verdelho and G. D. Marques, "Four-wire current regulator PWM voltage converter", IEEE Trans. on Ind. Electronics, Vol. 45, pp. 761-770, Oct. 1998.

[3] Richard Zhang, V. H.Prasad, D. Boroyevich, F.C. Lee, "Three-Dimensional Space Vector Modulation for Four-Leg Voltage-Source Converters," IEEE Trans. On Power Electronics, May 2002, Vol. 17, No. 3, pp. 314 326.

[4] Fang Zheng Peng, George W. Ott, Jr., and Donald J., "Adams Harmonic and Reactive Power Compensation Based on the Generalized Instantaneous Reactive Power Theory for Three-Phase Four-Wire Systems," IEEE Trans. On Power Electronics, Nov. 1998, vol. 13, No. 6, pp. 1174- 1181.

[5] Man-Chung Wong, "Research on The Parallel Power Qulaity Compensator for Three-Phase Four-Wire Systems", Ph. D. Thesis, Tsinghua University, Beijing, P. R. China, 2003.